# Nb$_3$Sn THIN FILM COATING METHOD FOR SUPERCONDUCTING MULTILAYERED STRUCTURE

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## Abstract

S-I-S (superconductor-insulator-superconductor) multilayered structure has been proposed in order to increase the maximum acceleration gradient of SRF cavities. Nb$_3$Sn is the material most expected as a superconducting layer of the S-I-S multilayered structure because it offers both a large critical temperature and large predicted H$_{sh}$.

Most important in fabricating Nb$_3$Sn thin films is the stoichiometry of the material produced, and the lack of tin leads to performance degradation. We have launched a new in-house DC magnetron sputtering apparatus for Nb$_3$Sn deposition. Nb and Sn layers were alternately and repeatedly deposited on Si wafer while adjusting the film thickness of each layer, so we successfully obtained Nb-Sn films having appropriate composition ratio. The as-deposited films were annealed under the temperature of 600 degree C for 1 hour to generate the Nb3Sn phase. The characteristics of Nb-Sn films evaluated by XRD, XRF, FE-SEM, and so on. We also measured critical temperature of the annealed films. In this paper, the detail of the Nb$_3$Sn coating method and the measurement result of the Nb-Sn films will be reported.

## INTRODUCTION

S-I-S thin film multilayered structure theory has been proposed to increase vortex penetration field of SRF cavities [1, 2]. According to this theory, the vortex penetration field of multilayered thin film structures can reach approximately 250 mT when NbN is used for the superconducting layer and approximately 480 mT when Nb$_3$Sn is used. However, it is not clear whether this calculated value in this theory can really be achieved, in fact, multilayered thin film cavities which exceed the maximum acceleration gradient of Nb cavities have not been realized. Thus, it is necessary to demonstrate the multilayered thin film theory and to establish coating techniques for fabricating S-I-S thin film multilayered cavities.

In order to demonstrate the theory, we firstly aimed to evaluate the effective H$_{c1}$ of S-I-S samples [3, 4]. In previous studies, we have already established the reactive sputtering conditions for obtaining high quality NbN thin films and have succeeded in fabricating S-I-S samples which consist of the various thickness of NbN layer, 30 nm SiO$_2$ layer, and pure Nb substrate. The XRD patterns of these S-I-S samples showed sharp Nb and NbN peaks [5]. As a result of effective H$_{c1}$ measurement of these NbN multilayer

samples, we clarified that the S-I-S structure have effective H$_{c1}$ higher than conventional Nb. In addition, it was experimentally proved that the optimum film thickness exists as theoretically predicted [6, 7].

In this study, we aim to fabricate Nb$_3$Sn thin films that are expected to achieve higher performance than NbN. However, the film formation of Nb$_3$Sn is more difficult and has many problems compared to NbN. Nb$_3$Sn may crack or peel off when used as a thin film because it is brittle. Moreover, in the case of depositing a film on the inner surface of the SRF cavity by sputtering method in the future, it is practically difficult to heat the cavity to a high temperature during deposition because a Sn target may be melted due to the radiant heat. In addition, since the Sn lack in the film leads to degradation of the critical temperature, a coating method that can appropriately adjust the composition ratio of Nb and Sn is required.

As a solution to all these problems, we have devised a method of laminating Nb and Sn alternately thinly and then post annealing at low temperature. The purpose of lowering the temperature of post annealing is to reduce the stress caused by the difference in thermal expansion coefficient between the substrate and the thin film and to suppress crystal grain growth. The key is to minimize the energy required for atomic diffusion by super-stacking the Nb and Sn layers in advance so that the Nb3Sn phase can be generated even at low temperature.

We newly launched an experimental sputtering apparatus for super-stacking of Nb and Sn alternately and a vacuum heat treatment furnace for post annealing of Nb-Sn thin films. In this report, the evaluation results of as-deposited and annealed Nb-Sn thin films are reported.

## EXPERIMENTAL DETAILS

### Sputtering Process

Our new experimental sputtering apparatus adopts inter-back system, and a substrate carrier on which 12 substrate holders capable of rotating and revolving are attached is transported to the sputtering chamber. Figure 1 shows the schematic diagram of the sputtering apparatus. The diameter of all the substrate holders are 4 inches. A maximum of four targets can be mounted to the sputtering chamber. This time, only Nb (RRR>300) and Sn targets are mounted for depositing Nb-Sn films. The sizes of both Nb and Sn targets are 5 inches by 10 inches. Since the substrate holders pass in front of the Nb and Sn targets while rotating and revolving, the sputtered Nb and Sn elements are uniformly and alternately deposited on substrates. The rotation speed
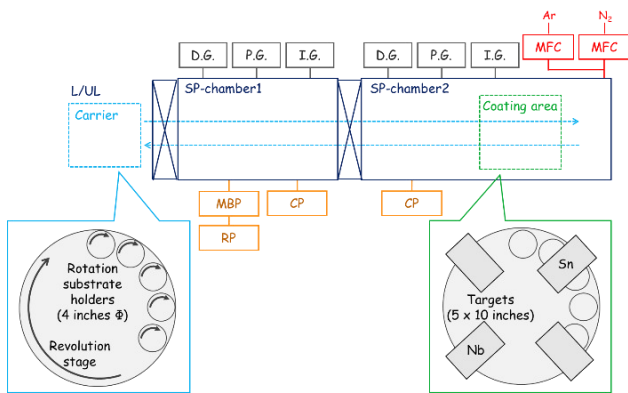
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Figure 1: Schematic diagram of in-house experimental sputtering apparatus.
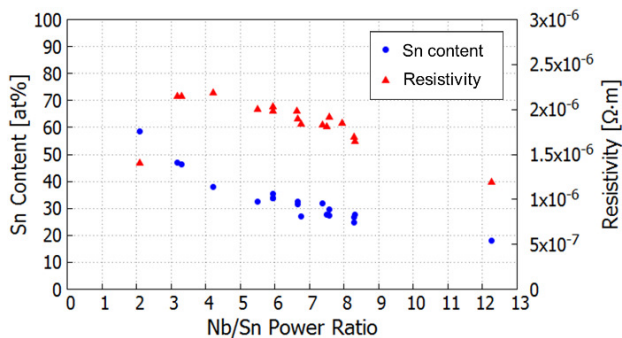


Figure 2: Atomic % Sn content and resistivity of Nb-Sn films for varying Nb/Sn input power ratio.

of the substrate holders is linked with the revolution speed which is freely adjustable. Therefore, it is possible to control the film thickness per one layer of Nb and Sn by adjusting the revolution speed. The Nb and Sn targets are powered by individual DC supply. The base pressure of the sputtering chamber is about $5 \times 10^{-4}$ Pa, and Ar pressure for discharge is adjusted to 0.6 Pa. The deposition temperature is room temperature.

At first, we investigated atomic % Sn content of as-deposited films while changing Nb/Sn input power ratio. The film resistivity of was also measured by four probe method. Figure 2 shows the correlation between atomic % Sn content and Nb/Sn input power ratio. It turned out that films with appropriate atomic % Sn content were obtained in the region of Nb/Sn power ratio about 5.9 to 8.3, so we prepared four samples deposited Nb-Sn on Si wafer under the condition of this Nb/Sn power ratio, and post annealing was performed. The film thickness of each sample is about 300 nm. Table 1 shows the Sn atomic % content of these samples measured by XRF.

### Post Annealing Process

The as-deposited Nb-Sn films were annealed by using an in-house vacuum heat treatment furnace. The ultimate pressure of the furnace was less than $1 \times 10^{-4}$ Pa. Nb-Sn samples were placed in a high purity Ti box and heat treated. The annealing temperature was 600 degree C for 1 hour. The samples were taken out after the temperature of the sample spontaneously decreased less than 50 degree C,

Table 1: Sn Atomic % Content of Samples A to D

| Sample Name | Nb/Sn Input Power Ratio | Sn Content [atomic %] |
|---|---|---|
| A | 5.9 | 33.8 |
| B | 6.6 | 31.4 |
| C | 7.6 | 29.6 |
| D | 8.3 | 27.5 |

so we consider that there was no oxide layer on the surface of the samples.

### $T_c$ Measurement

The critical temperature of the annealed Nb3Sn samples were measured by four probe method. The distance of between terminals of the voltage probe was 90 mm, and the width of the samples were 30 mm. The current value for measurement was set to 1 mA. The temperature of samples was measured by directly contacting the sample with a thin film resistance cryogenic temperature sensor calibrated with an Nb bulk standard sample.

## RESULTS AND DISCUSSION

Figure 3 shows the measurement result of XRD of as-deposited Nb-Sn film samples. Samples A to D are identical to those listed in Table 1. Broad peaks which is considered to be a mixed peak of Nb and Sn are observed in all samples. Figure 4 shows the XRD patterns of annealed $Nb_3Sn$ film samples A to D. XRD patterns of all the samples indicate $Nb_3Sn$ phase, and only the sample D also indicates the peak considered to be Nb. However the all peaks are slightly shifted to the lower angle side. We consider that the lattice was distorted and the interatomic distance was increased because extra atoms were taken into the $Nb_3Sn$ lattice or the Sn concentration in the lattice was not optimum. The higher the concentration of Nb, the shorter the FWHM of the $Nb_3Sn$ peak and the better the crystallinity are. But if the Nb concentration is too high, Nb phase remains. At present, since the crystallinity of the $Nb_3Sn$ phase is not very good, we need to optimize the sputtering conditions and annealing conditions in the future.

Figure 5 shows the SEM cross-section images of annealed $Nb_3Sn$ film samples A to D. The surfaces of the obtained $Nb_3Sn$ films on Si wafer are very smooth except for the sample C. This is because grain growth was suppressed by adopting the super-stack sputtering method and the low annealing temperature. However, hillocks, which are protrusions generated to locally relieve internal stress in thin film, are seen in samples A and D. This is undesirable because it causes deterioration of the surface roughness of the film, so further stress reduction may be necessary. Figure 6 shows the $T_c$ measurement result of the annealed $Nb_3Sn$ film samples A to D. Table 2 shows the critical temperature (onset). We confirmed the superconducting transition in all the samples. The samples C and D indicated higher critical temperature than Nb. Therefore, we consider that the $Nb_3Sn$ phase is definitely generated even if at low annealing temperature. However, the critical temperature of any
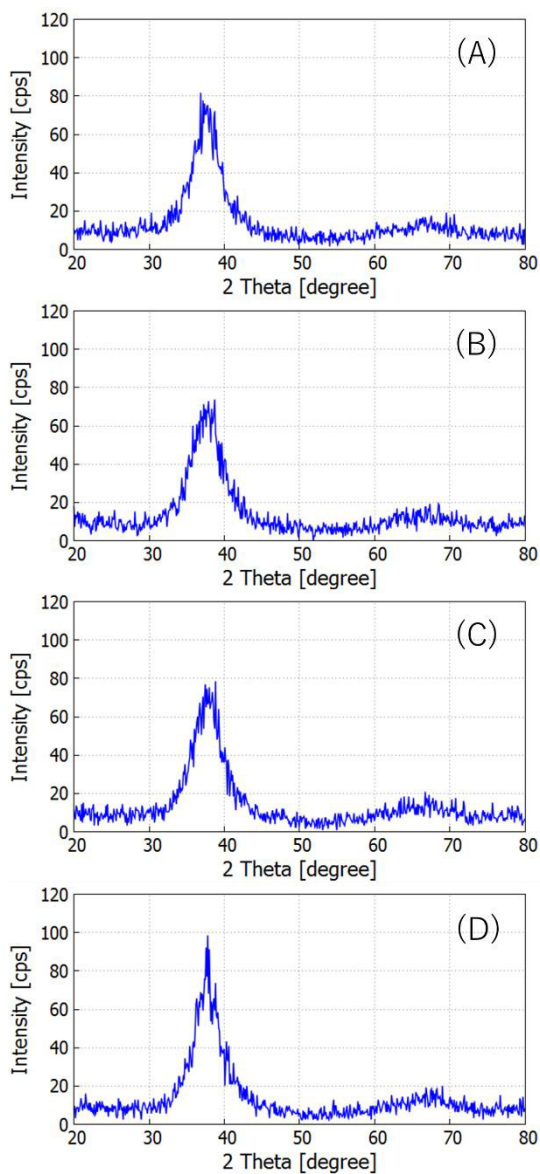
Figure 3: XRD patterns of as-deposited Nb-Sn samples A to D.

Figure 4: XRD patterns of Nb$_3$Sn samples A to D annealed at 600 degree C.

samples is lower than ideal value of Nb$_3$Sn (18K) because the crystallinity of the Nb$_3$Sn films is not very good. The samples C and D had superconducting transition in two step. We consider that Nb phase remaining in films causes this second transition.

The film stress of the superconducting layer is also influence to the value of the critical temperature. The Nb$_3$Sn phase is generated on Si wafer when the temperature of Si substrate is 600 degree C. After that, the Nb$_3$Sn film and the substrate shrink when cooled to room temperature, but a mismatch caused by the difference in thermal expansion coefficient between the film and the substrate, and thermal stress occurs. We consider that the film stress can be reduced if we use another substrate, for example Nb. In addition, Selection of an appropriate insulating layer for reducing the stress is very important when fabricating an S-I-S sample.
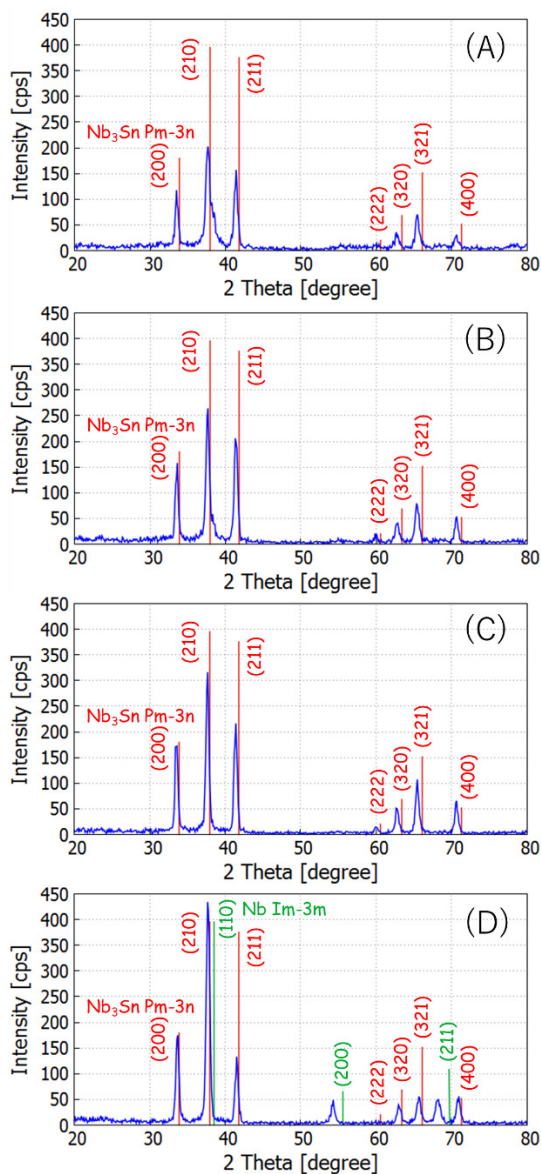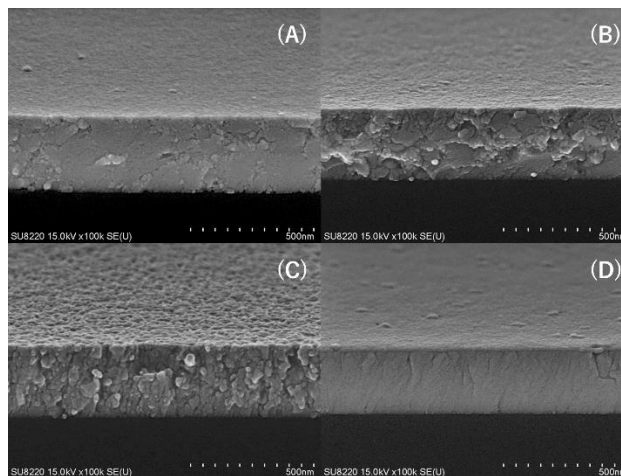
Figure 5: SEM cross-section images of Nb$_3$Sn samples A to D annealed at 600 degree C.
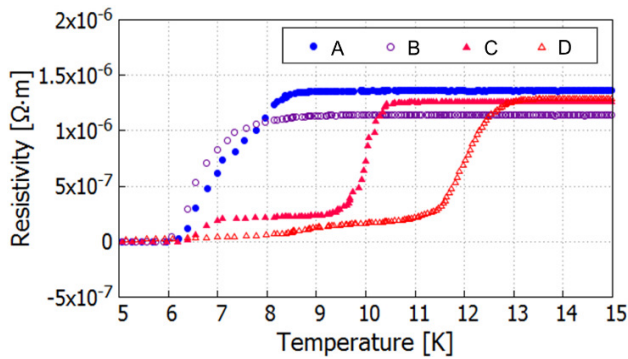
Figure 6: Result of $T_c$ measurement of $Nb_3Sn$ samples A to D annealed at 600 degree C.

Table 2: Critical Temperature of Samples A to D

| Sample Name | Nb/Sn Input Power Ratio | Critical Temperature [K] |
|---|---|---|
| A | 5.9 | 8.25 |
| B | 6.6 | 7.30 |
| C | 7.6 | 10.40 |
| D | 8.3 | 12.66 |

## CONCLUSION

We successfully generated $Nb_3Sn$ single phase thin films by super-stacking sputtering method and post annealing at low temperature of 600 degree C. The surface of the obtained $Nb_3Sn$ thin films on Si wafer was very smooth. This is because the crystal grain growth was suppressing by lowering annealing temperature. However, from the measurement results of the XRD peaks and the critical temperature, we consider that the crystallinity of the $Nb_3Sn$ films is not very good yet. In the future, we will optimize the sputtering conditions and the annealing conditions, and aim to fabricate $Nb_3Sn$ thin films with high critical temperature. In addition, we plan to prepare $Nb_3Sn$-insulator-Nb multilayered samples and measure the vortex penetration field of that samples.

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