

MODERN DIGITAL SYNCHRONIZATION SYSTEM FOR LARGE PARTICLE ACCELERATORS

G. Fatkin*, A. Senchenko, M. Vasilyev, Ya. Macheret BINP and NSU, Novosibirsk, Russia
A. Selivanov BINP, Novosibirsk, Russia

Abstract

The review of modern approach to synchronizing large physical installations including accelerators is given in this paper. This approach is based on using digital modules connected by an optical link to transfer a mixed clock/data signal. A sub-nanosecond jitter and nanosecond resolution can be achieved this way as well as dynamic delay compensation and precision timing. Several modern synchronization systems based on this principle are discussed: White Rabbit, MRF, J-PARC and BINP developments.

INTRODUCTION

In recent years the approach to the synchronization of large physical installations has drastically changed. With new developments in digital electronics and optical technologies transferring a signal including carrying frequency and encoded data over a distance of several kilometers became possible. Using them a scheme was devised that allows to achieve an unprecedented precision, flexibility and range for synchronisation of multitude control stations. This scheme allows to synchronize multitude of devices over the distance of multiple kilometers with jitter less than 100 fs.

A range of systems based on these principles were developed and are used in physical installations around the world. Most notable of them are: The White Rabbit Project (CERN) [1] which is planned for use in ESRF, SKA and several other installations; Micro-Research Finland (MRF) timing system [2] that is used in NSLS, Libera, ELI, and FRIB; J-Parc timing system [3] and Greenfield Technology timing system [4] used in Soleil, AWE, etc. This approaches were also recently used in synchronisation system of LIA-20 accelerator [5] in a system developed at BINP. Now let us describe the principles of their operation.

SYNCHRONISATION SCHEME

For the sake of simplicity let us let us consider two nodes, each of them functioning as a clock. By clock we mean a counter working on a specific stable frequency. The synchronization of two clocks then consists of several procedures:

- syntonisation – equalizing the frequencies;
- tuning of the phases;
- synchronizing the counter values;

In practice one of this clocks typically with a better frequency source such as a rubidium oscillator, or GPS-transmitted atomic clock frequency is considered a master-clock, and other one is a slave-clock.

* G.A.Fatkin@inp.nsk.su

Let us first consider the syntonization of these two clocks. The general idea between all of the modern synchronisation systems is shown on Fig. 1. In the master module the frequency from the master clock is mixed with data using an encoder. Then the produced clock/data signal from encoder is fed through an optical transmitter (TX) to an optical line. On a slave module the optical signal is converted to an electric one by a receiver (RX) and is fed to a clock data recovery scheme (CDR). Basically this scheme consists of a phase-locked loop that locks onto a frequency and provides it further to a module and a data recovery circuit. The data recovery circuit is more complicated and we will not discuss it in this article, but generally it performs a decoding operation based on the incoming clock/data signal and a frequency obtained by PLL.

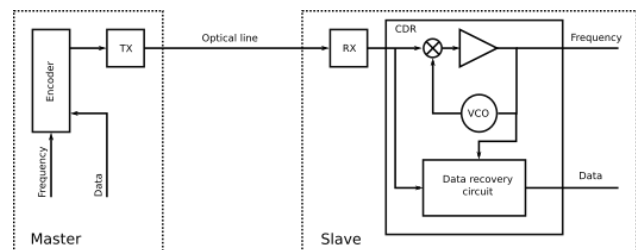


Figure 1: Synchronisation scheme.

The PLL is a central element in this scheme that determines the quality of the frequency tracking. A received frequency from PLL is strictly locked to a transmitted master frequency, and with modern PLL's the accuracy in order of tens of picoseconds is attainable with ease. It should be noted also that the PLL can be used to create a frequency that is in a rational ratio to its input. This can be convenient in cyclic machines and is used to obtain an RF from master frequency source.

The ability to transmit data using this scheme is utilized to synchronously transfer the messages. This messages can contain delay and phase difference measurements as well as command sequences.

To measure the transmission delay between the following procedure is used: master module sends a special message to the slave module which sends back a reply immediately after receiving. Master module measures the time necessary for the transfer and thus gets a double transmission delay. There are some problems with this method if you want to achieve an accuracy better than several nanoseconds, because in general the transmission line is assymetric, thus Master-Slave and Slave-Master delays can be different. To solve this problems an elaborate calibration schemes are used. After the Master-Slave delay is measured it can be transmitted to a slave module to be used

Content from this work may be used under the terms of the CC BY 3.0 licence (© 2018). Any distribution of this work must maintain attribution to the author(s), title of the work, publisher, and DOI.

for a periodical delay compensation.

PHASE TUNING

Practically achievable frequencies for transfer through fiber-optic are: 1.2 - 2.4 GHz. Thus the actual quantum of synchronization is not less than 416 ps. As all of the digital schemes have inherent quantization noise not less than the value of a quantum, to achieve better synchronisation a special methodics for phase measurements and is needed. There is a methodic called Digital Dual Mixer Time Difference or DDMTD for this [6]. The principle of this scheme is shown on Fig. 2.

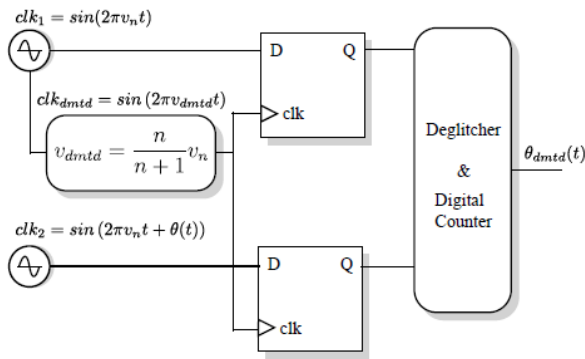


Figure 2: DDMTD scheme.

In our opinion, this scheme could be viewed as a stroboscopic measurements. If we need to measure the phase difference between two signals clk_1 and clk_2 with the same frequency v_n , we need to generate a slightly offset frequency v_{dmdt} . Then, strobing both signals with this offset frequency we effectively stretch the signals in time by the same ratio. After that, the counter with a standard XOR phase measurement scheme could be used to achieve a great precision of phase measurements of around 1 ps or less.

This scheme is used in synchronization systems as following. The clock signal is transferred to the slave module and then it is fed back to the master module. In master module a DDMTD is used to measure the phase and then these measurements are transferred back to the slave module which adjusts it's phase accordingly using PLL. Overall accuracy achieved using this scheme is around 10 ps between modules.

COUNTER ADJUSTMENT

After the syntonization and phase adjustment are finished the values in the counters of different modules must be aligned. Several different methods are used to accomplish this task. Firstly, some systems like MRF, SuperKEK and Greenfield don't do this at all. Thus you have a synchronized and synphazed counters each counting on it's own.

Secondly, the precision time protocol (PTP) [7] protocol can be used for this task with special modifications required for greater accuracy. These modifications were made by White Rabbit team (CERN) and were added to

the PTP standard. The basic idea of PTP is shown on fig. 3. Two modules are exchanging messages, containing local time of sending (t_1, t_3), and record local time of receiving (t_2, t_4). The link delay than can be determined as $\delta = \frac{(t_4 - t_1) - (t_3 - t_2)}{2}$. and clock offset as $x = t_2 - t_1 + \delta$. Thus after several such exchanges you can derive the mean values of link delay and clock offsets. After that two commands "plus tick" and "minus tick" are used to bring this slack to zero.

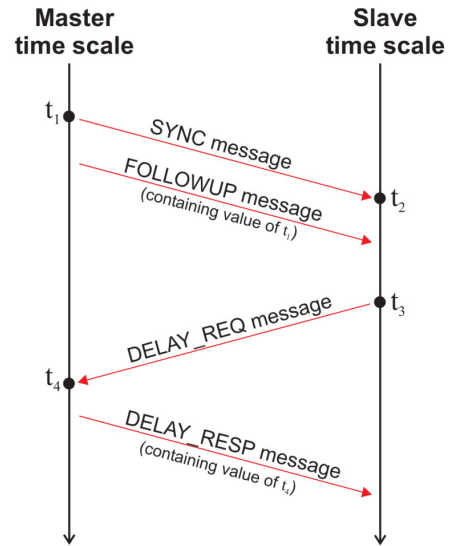


Figure 3: PTP procedure.

We should note that PTP protocol was introduced to synchronize nodes with different feeding frequencies, that periodically need to be co-aligned, such as personal computers. If the frequency of all of the nodes is the same then this approach seems to be a great overhead. Thus we introduced a synchronous counter adjustment procedure for our system at BINP. It is shown on Fig. 4.

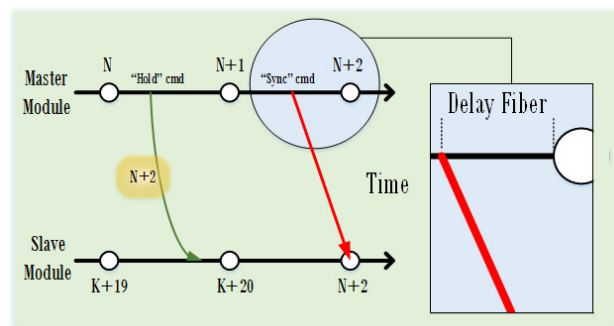


Figure 4: Synchronous counter adjustment procedure.

The basic idea beneath the procedure is to transfer the message with a future time from master beforehand and set this time to the counter of the slave and stop it. After that the "Start" command is given in specific time taking all delays into account, and the slave counter starts working

Table 1: Existing Synchronization Systems

Name	Frequency range	Precision	Compensation	Common clock	Event transfer
White rabbit	125 MHz	< 10 ps RMS	Phase, Delay	PTP	Soft-synchronous
MRF Timing	50 - 142.9 MHz	< 10 ps RMS	Phase, Delay	No	Synchronous
Greenfield Timing	80 MHz	< 10 ps RMS	Phase	No	Synchronous
J-PARC	96 MHz	30 ps?	No	No	Synchronous
BINP	50 - 125 MHz	< 50 ps RMS	Phase, Delay	Yes	Synchronous

completely synchronous with the master. As the frequency is essentially the same, no tuning will be needed after this procedure and it has to be done only once after connecting the node to the timing network.

EXISTING IMPLIMENTATIONS

Now let us discuss some of the details of the existing synchronization systems. The Table 1 is presented with a comparison of the abovementioned systems. Unfortunately, it is not easy to collect the information about some of these systems, thus this table may contain some errors.

Let us now discuss some of the properties of this systems. First of all we will describe White Rabbit timing system. It is an open-hardware project developed at CERN. It is based on using synchronous ethernet and PTP protocols. Essentially it provides a common 125 MHz clock with very high precision on several nodes over the distance of several kilometers. Also it provides a synchronous ethernet network, using which you can develop an arbitrary data transfer schemes. We should note that as it is essentially an ethernet, “hard” synchronisation is not possible at all, because the message arrival time depends on many factors such as network load etc.

We will not discuss here Greenfield and J-PARC solutions, because they are in many aspects similar to the MRF timing system. So, let us discuss the MRF Timing solution. It is based on transferring an arbitrary clock in a wide range and provide a synchronous messaging on this clock. This allows to use this clock to feed the low-level RF generators. To provide “hard” synchronization a prioritisation scheme for the messages is implimented. In recent years digital delay and phase compensation were added. Generally, the MRF system doesn’t provide “common time”, it only provides transferring the event signals through the network.

And finally we will talk a little about the system designed at BINP, which is discussed in detail at [5]. Our system combines the “common clock” and “hard” synchronization events approaches to achieve the same accuracy goals as other systems. It also allows wide frequency range to alleviate its use in LLRF synchronization. It is already successfully used on LIA-5 accelerator and is planned for use in several other projects.

CONCLUSION

The synchronization systems based on the principles that are described in this article are introduced for most of the modern accelerator and big physics installations. As several “megascience” projects are being developed in Russia, the usage of such a system in them seems to be inevitable.

REFERENCES

- [1] J. Serrano, P. Alvarez, M. Cattin, E. G. Cota, P. M. J. H. Lewis, T. Wostowski et al. , The White Rabbit Project, in Proceedings of ICALEPCS 2009 TUC004 , Kobe, Japan.
- [2] Micro-Research Finland: <http://www.mrf.fi>
- [3] F. Takamura, H. Yoshikawa, J. Chiba, M. Yoshii, M. Tanaka, S. Shimazaki, “J-PARC Timing System,” in Proceedings of ICALEPCS 2003 TU115, Gyeongju, Korea.
- [4] D. Monnier-Bourdin, B. Riondet, S. Perez, “Picosecond Timing System,” in Proceedings of ICALEPCS 2013 THPPC090, San Francisco, CA, USA
- [5] Ya. Macheret, A. Selivanov, G. Fatkin, M. Vasilyev, “development of Modern Digital Synchronization Modules at BINP”, THCP10, these proceedings
- [6] P. Moreira, P. Alvarez, J. Serrano, I. Darwezeh, “Digital Dual Mixer Time Difference for Sub-Nanosecond Time Synchronization in Ethernet” , 2010 IEEE Frequency Control Symposium.
- [7] IEEE Standard for a Precision Clock Synchronization Protocol for Networked Measurement and Control Systems, IEEE Std. 1588-2008, 2008.