

**BUILDING  
CONTROL SYSTEM  
REMOTELY**

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**BUILDING  
CONTROL SYSTEM  
REMOTELY**

100 Hz 10 J

LASER

HiLASE

CLF

**EPICS**

**30+ IOCs**

**500+ PVs**

**BUILDING  
CONTROL SYSTEM**

**REMOTELY**

**DEVICE**

**MANUFACTURER**

**DOCUMENTATION**

**USER MANUAL**

**TRAINING**

**TESTS**



**LAB**

**IOC  
USER INTERFACE  
TESTS**

# **MANUFACTURER**

**DOCUMENTATION  
MANUAL  
TRAINING  
TESTS**

# **LAB**

**IOC  
USER INTERFACE  
TESTS**

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MANUAL  
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# LAB

IOC  
USER INTERFACE  
TESTS

**COMMUNICATION**

**SIMULATE**

**OFF THE SHELF**

**KNOWN ALREADY  
OFF THE SHELF**

**NEW**

**KNOWN ALREADY**

**OFF THE SHELF**

**SIM**

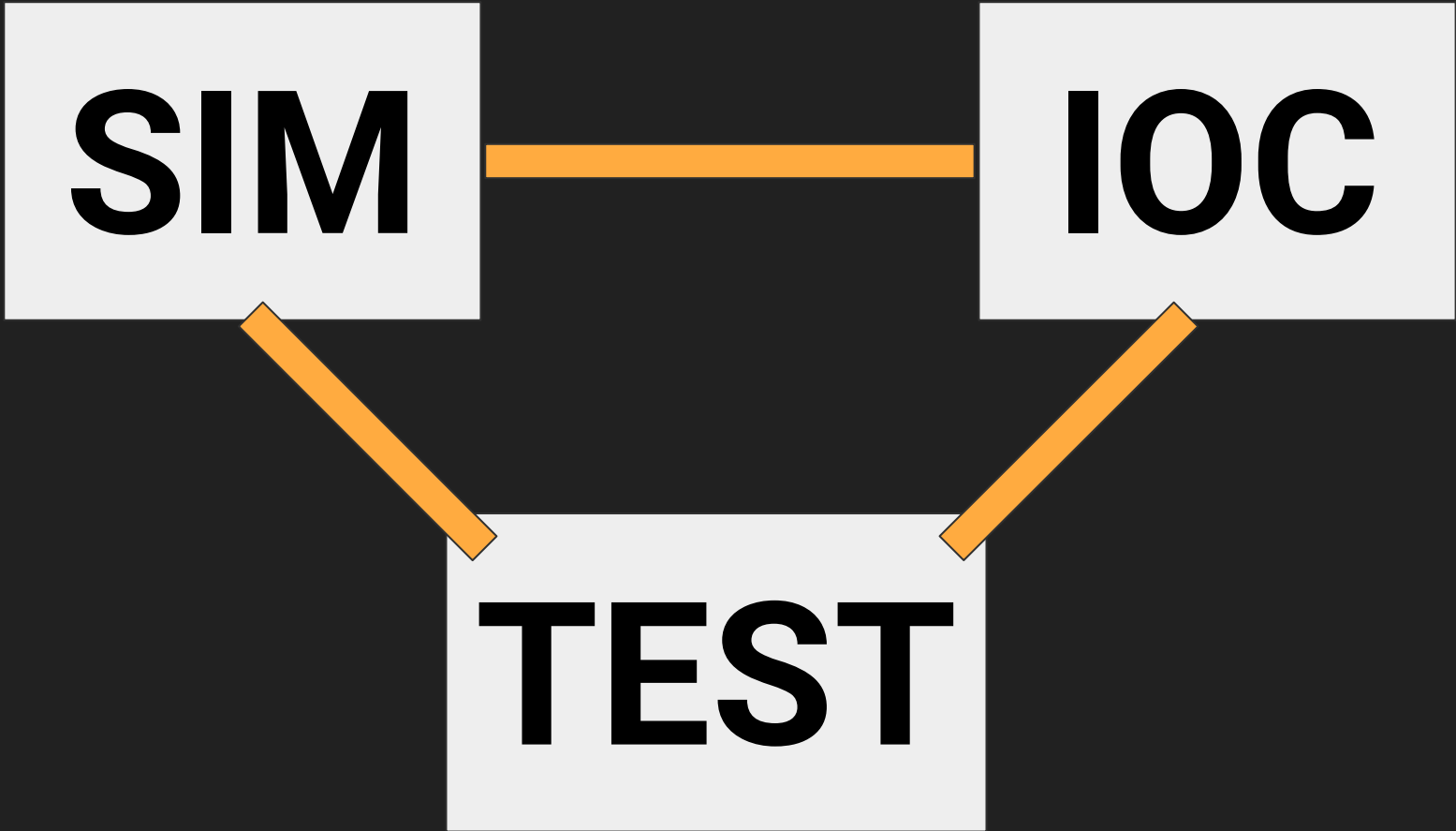
**IOC**



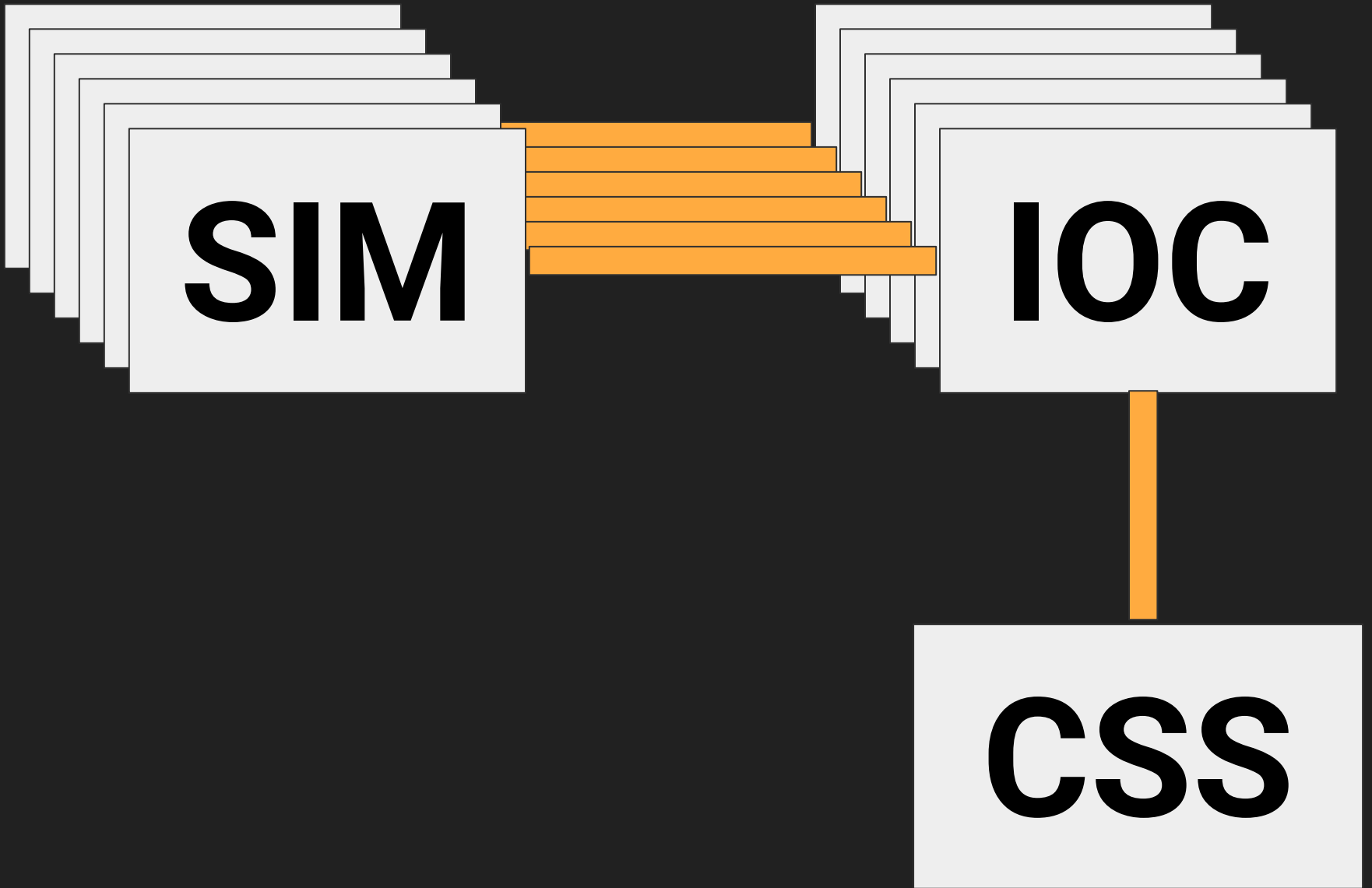
**SIM**

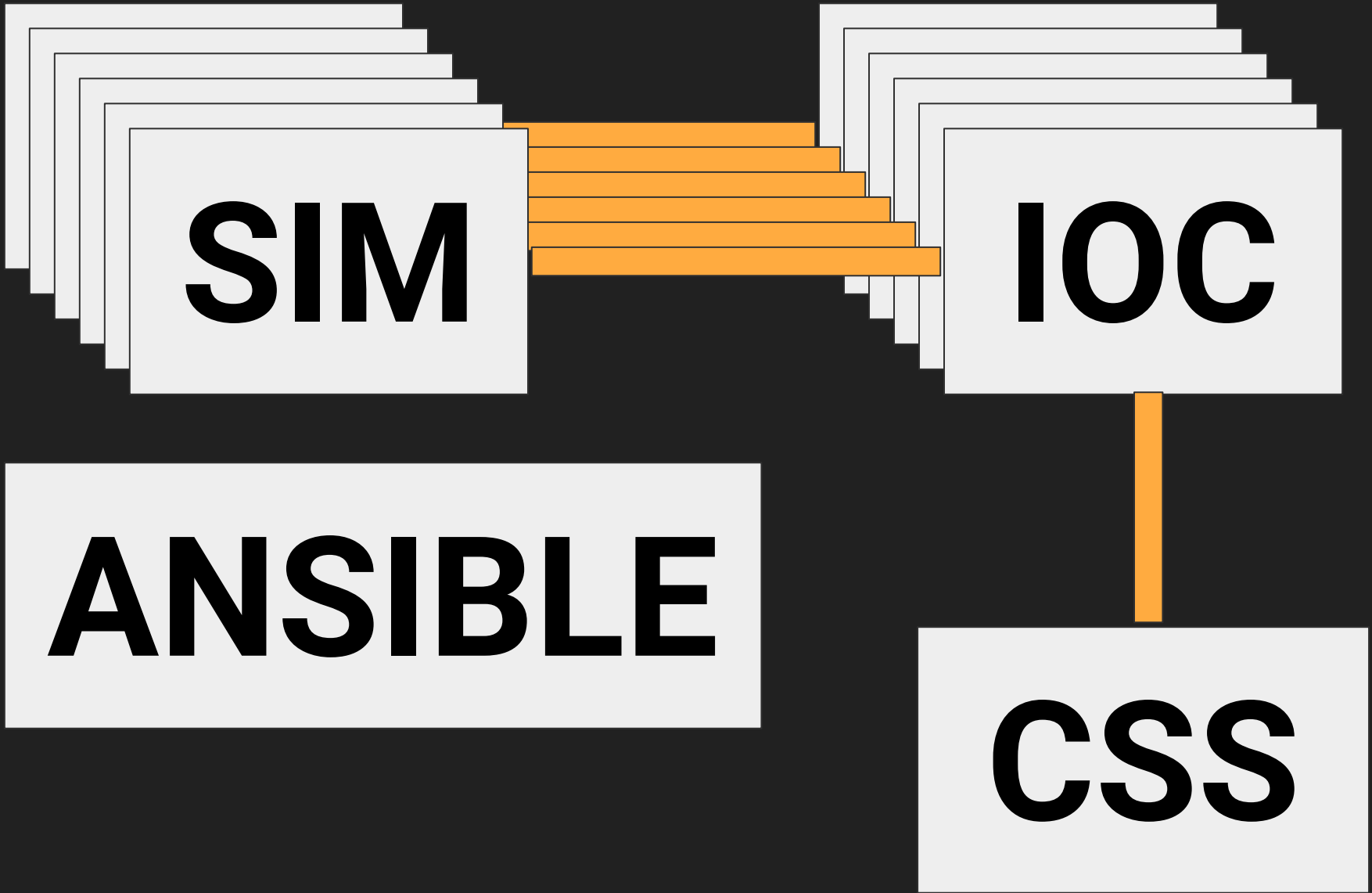
**IOC**

**TEST**



**STAGING**





**SIM**

**IOC**

**ANSIBLE**

**CSS**

**SIM**

The diagram features two stacks of white rectangular cards. The left stack is labeled 'SIM' and the right stack is labeled 'IOC'. Five horizontal orange lines connect the two stacks. Below the 'SIM' stack are two stacked white boxes labeled 'ANSIBLE' and 'GRAFANA'. Below the 'IOC' stack is a white box labeled 'CSS', connected to the 'IOC' stack by a vertical orange line.

**IOC**

**ANSIBLE**

**GRAFANA**

**CSS**

Device Connected

CO-LASER-RACK Connected	CO-SCOPE Connected	FE-D-EM-1 Connected	FE-PA1-CHILLER Connected
FE-PA1-DELAY-GEN Connected	FE-PA1-DIODE-DRIVER Connected	TJ-PD Connected	

Monitored PVs <b>56</b>	Connected PVs <b>56</b>
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Start Time

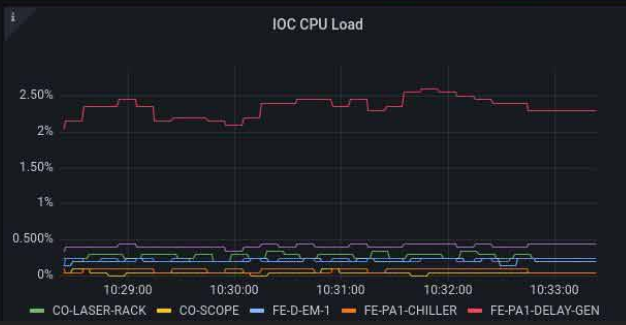
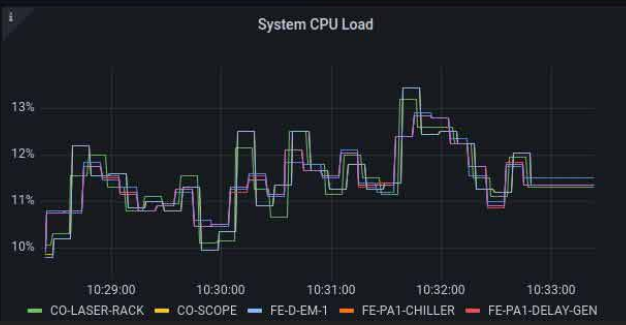
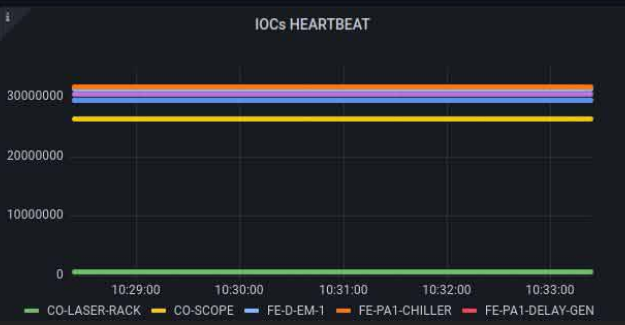
CO-LASER-RACK 2022-09-11 21:09:41	CO-SCOPE 2021-11-19 10:58:00	FE-D-EM-1 2021-09-21 12:37:04	FE-PA1-CHILLER 2021-09-17 13:57:55
FE-PA1-DELAY-GEN 2021-10-13 14:56:30	FE-PA1-DIODE-DRIVER 2021-10-12 20:05:08	TJ-PD 2021-10-01 16:38:23	

Up Time

CO-LASER-RACK 7 d 13:23:11	CO-SCOPE 303 d 22:34:52	FE-D-EM-1 362 d 21:55:47	FE-PA1-CHILLER 366 d 20:34:57
FE-PA1-DELAY-GEN 340 d 19:36:23	FE-PA1-DIODE-DRIVER 341 d 14:27:45	TJ-PD 352 d 17:54:29	

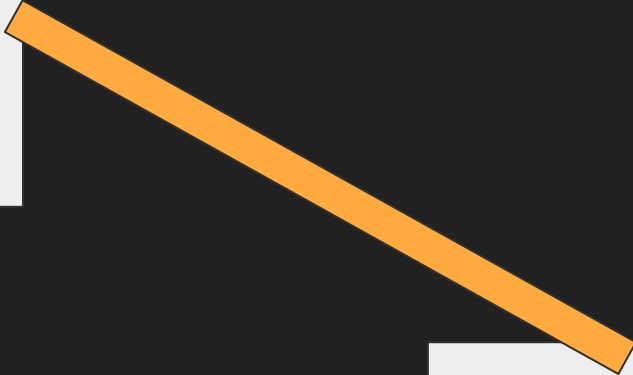
IOC Memory Usage

CO-LASER-RACK 73.7 MB	CO-SCOPE 112 MB	FE-D-EM-1 70.7 MB	FE-PA1-CHILLER 71.2 MB
FE-PA1-DELAY-GEN 76.1 MB	FE-PA1-DIODE-DRIVER 77.2 MB	TJ-PD 72.9 MB	



**TEST**

**TEST**



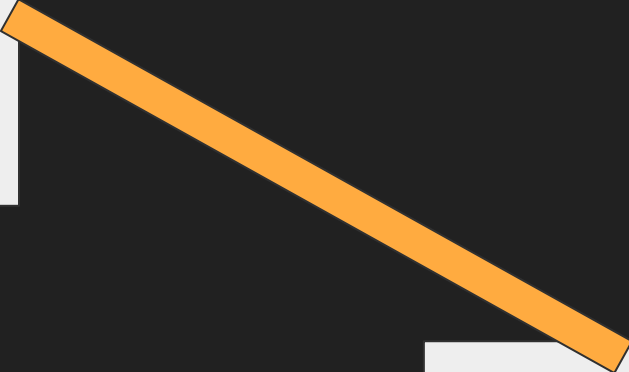
**STG**



**TEST**

**STG**

**LAB**



# SUMMARY

**MITIGATE**

**RISKS**

**MISTAKES  
ARE  
OKAY**

**SIMULATE**

**TEST**

**RUN IN**

**STAGING**

**VISIT**

**THE LAB**

**THANK**

**YOU!**



