Next Generation GSI/FAIR Scalable Control Unit

Lessons Learned from 10 years in the field

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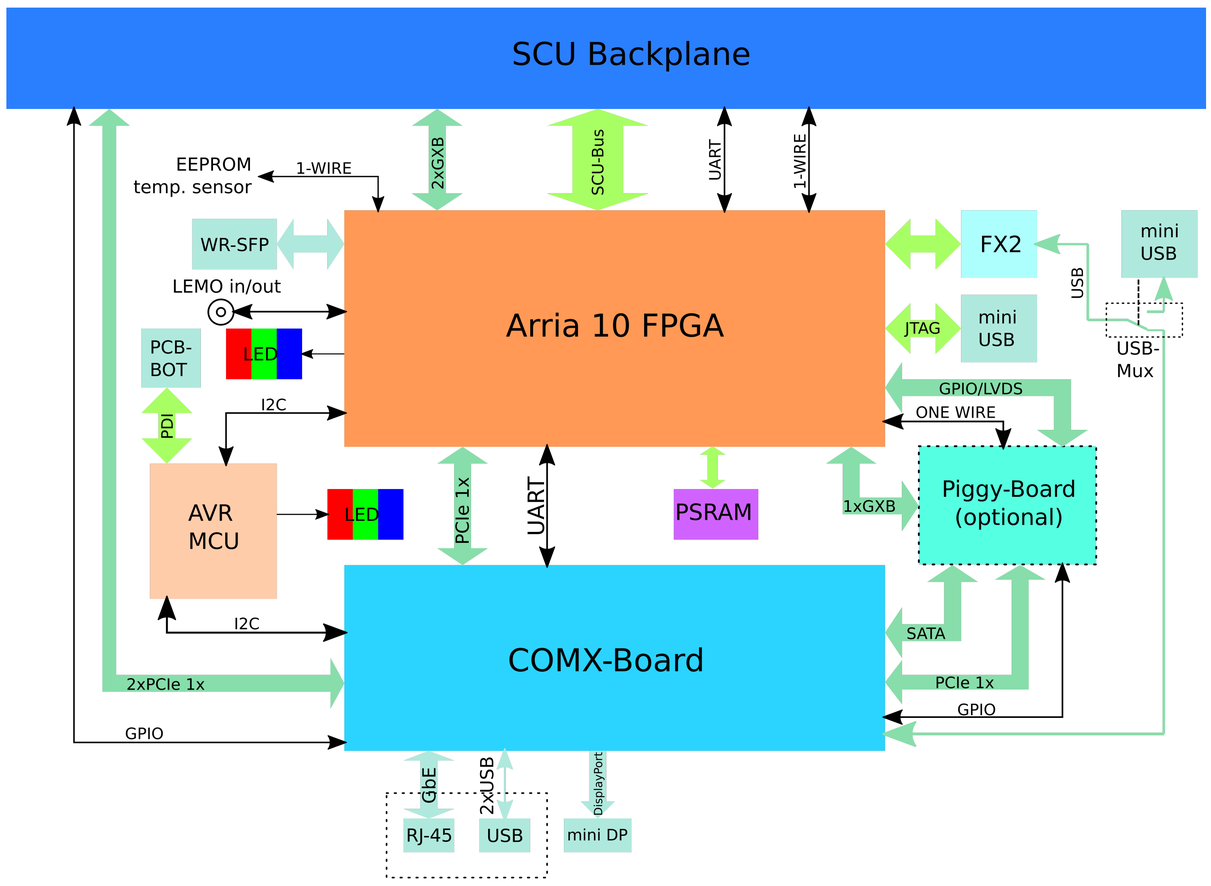
Abstract

The end-of-life of many components brought the need for a redesign of our main Control System Front-End - the SCU (Scalable Control Unit). It was a chance to make improvements and use more powerful state-of-the-art core components. This included a new Arria 10 FPGA and a completely redesigned housekeeping circuit based on an AVR microcontroller. Further, the project was cleaned by removing unused components and features. Main frame conditions stay fixed for backward compatibility, like the mechanical form factor or the 16-bit parallel bus. Majority of gateware and firmware could be reused and just some adaptations for the new FPGA were needed. Nevertheless, providing continuous compatibility with legacy peripherals needed a substantial effort.

Scalable Control Units (SCUs)

- Uniform, intelligent, realtime interface to accelerator hardware
- Gigabit Ethernet, White-Rabbit timing
- Custom baseboard with Intel Arria FPGA
- Off-the-shelf COMX computing module
- Linux OS, diskless

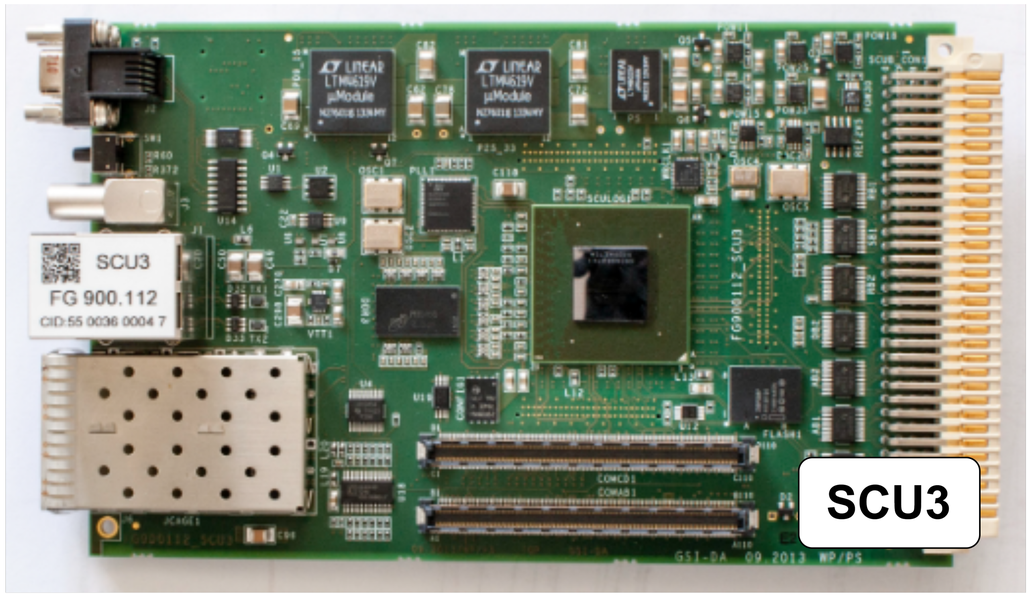
SCU4 Hardware Design



FPGA properties

Parameter	SCU3	SCU4
FPGA Type	Arria II	Arria 10
Technology	40 nm	20 nm
Logic Elements	100 k	270 k
BlockRAM	8121 Kb	17452 Kb

SCU4 vs SCU3

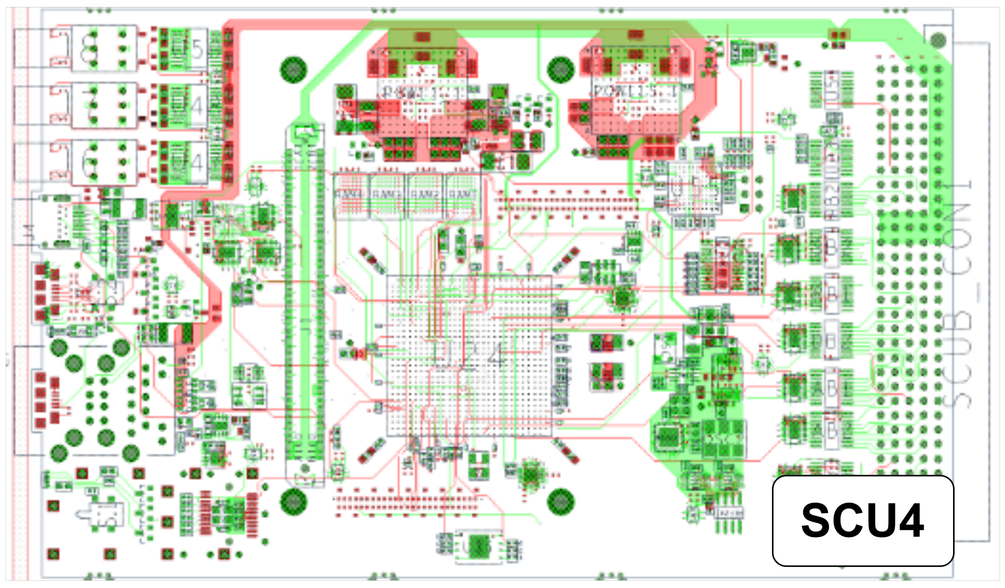


Removed
2nd SFP Cage
2x Serial Port
CFI Flash

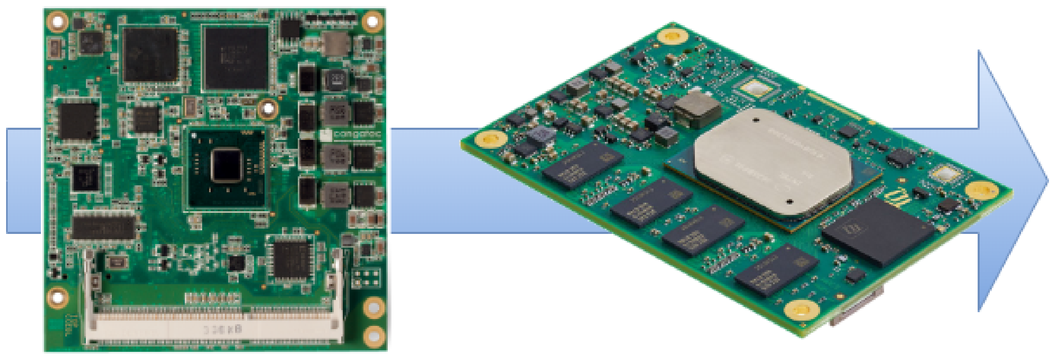
Added
USB-Device
DisplayPort

Changed
2x LEMO IO → 2 In / 4 Out
DDR RAM → PSRAM
Arria II → Arria 10

Kept
GigE Ethernet
2x USB Host
SCU-Bus



Computing Modules



COMX Computing module

Feature	SCU3	SCU4
Form Factor	COM Express Type 2	COM Express Type 10
CPU	Intel N2600	Intel E3940
Cores	2 (4 HT)	4 (native)
CPU speed	1.6 GHz	1.8 GHz
RAM size	4 GB	8 GB
Geekbench 5.0		
Single-Core Score	89	285
Multi-Core Score	238	1065

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