NEXT GENERATION GSI/FAIR SCALABLE CONTROL UNIT: LESSONS LEARNED FROM 10 YEARS IN THE FIELD

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Abstract

The end-of-life of many components brought the need for a redesign of the main Control System Front-End for GSI accelerators - the SCU (Scaleable Control Unit). It was a chance to make improvements and use more powerful stateof-the-art core components. This included a new Arria 10 FPGA and a completely redesigned housekeeping circuit based on an AVR micro controller. Further, the project was cleaned by removing unused components and features. Main frame conditions stay fixed for backward compatibility, like the mechanical form factor or the 16-bit parallel bus. Majority of gateware and firmware could be reused and just some adaptations for the new FPGA were needed. Nevertheless, providing continuous compatibility with legacy peripherals needed a substantial effort.

INTRODUCTION

Scaleable control units (SCUs) have been designed as a uniform, intelligent, realtime interface between various electronic components of accelerators and the control network. Internally, they contain an off-the-shelf computing module (main CPU, main memory) running Linux and a custom baseboard (I/Os, White-Rabbit timing receiver) with an Intel Arria FPGA as summarized in Table 1. The integrated timing receiver allows executing various tasks with nanosecondlevel precision while the main CPU covers higher-level computing and data management. On the network side, they offer a Gigabit Ethernet interface for communications and a White-Rabbit slave for timing and triggering. On the device side, they are equipped with a parallel bus and some further interfaces as shown in Fig. 1. The device is disc-less: all data, software and the boot image are delivered via the network.

The new generation, the SCU 4, keeps compatibility with previous versions while providing significantly more resources.

SCU4 HARDWARE DESIGN

Table 1: FPGA Comparison

Parameter	SCU3	SCU4
FPGA Type	Arria II	Arria 10
Technology	40 nm	20 nm
Logic Elements	100 k	270 k
BlockRAM	8121 Kb	17 452 Kb

The general design was inherited after the previous SCU generation [1]. The basic parameters like mechanical dimen-



Figure 1: Block diagram of SCU4.

sions and electrical connection to the back-plane remained unchanged.

Major changes took place regarding the front panel. An OLED-display was removed. It turned out to be of limited use while it needed significant effort in assembly and occupied valuable space. Instead, a DisplayPort socket was added which allows connecting an external screen and a RGB-LED indicates the system status.

An important feedback from field operation was the lack of User-I/Os. As a result we added four additional user I/O lines. A dual mini D-Sub 9 debug connector was replaced by a mini USB device connector. A summary of these changes is shown in Table 2.

Table 2: SCU IOs

IOs	SCU3	SCU4
SCU-Bus	1	1
SFP	2	1
GbE Ethernet	1	1
USB 2.0 Host	2	2
USB 2.0 Device	-	1
Serial	2	_
Video	-	miniDP
LEMO 5V-TTL	2 In/Out	2 In, 4 Out
Logic-Analyser	1	—

The form-factor of the computing module has been changed from COMX Type 2 to Type 10 [2]. With a smaller footprint, it allowed us to rotate the module by 90 degrees, giving better airflow to cool the FPGA. The new module brings also advantages in processing power, as shown in Table 3.

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Figure 2: Top Layer: Red marked areas need for $1.8 V \leftrightarrow 3.3 V$ levelshifting (including device, keep-up and vias).

The communication between the main CPU and the FPGA is still done via PCIe. However, an additional connection via USB is provided, which offers shorter latency in case of single Byte/Word access operations.

Further, the external FPGA memory was updated. A CFI-Flash memory was removed as it was never used with the SCU3. The external FPGA DDR memory was replaced by a pseudo-SRAM. This has advantages for the FPGA pinning and synthesis and allowed reducing the number of power supply voltages.

Feature	SCU3	SCU4	
Form Factor	COM Express	COM Express	
	Type 2	Type 10	
CPU	Intel N2600	Intel E3940	
Cores	2 (4 HT)	4 (native)	
CPU speed	1.6 GHz	1.8 GHz	
RAM size	4 GB	8 GB	
Geekbench 5.0			
Single-Core Score	89	285	
Multi-Core Score	238	1065	

One big difference between the Arria II and that Arria 10 is the Arria 10 cannot use 3.3V as I/O-Voltage anymore. On the other hand, a lot of legacy features need 3.3V voltage levels. This makes it necessary to add $1.8V \leftrightarrow 3.3V$ levelshifters. In our case this requires nearly 7 percent of the PCB space as shown in Fig. 2.

VOLTAGE LEVELS AND POWER

The SCU has rather complicated power supply scheme, as shown in Fig. 3. To simplify the power supply, we decided to use a FPGA speed grade with the same voltage level for the core and the transceiver and just one voltage level for I/O. Using only 1.8 V as I/O voltage prevents the use of modern DDR-RAM as external memory.

The Arria 10 needs a special power sequence. This is provided by an ATxmega MCU-based circuitry. The MCU is also used for additional housekeeping tasks. In the early



stage, a MAX 10 FPGA was planned for this job. Unfortunately, supply-chain issues brought the need to switch to an easier available chip.

PARALLEL AND SERIAL BUSSES

The main purpose of the SCU is the provision of the SCU bus. It is a 16-bit parallel backplane bus with 12 slots for slave cards. These slave cards come in a variety of types like ADC/DAC, GPIO, MIL-STD1553 master, controllers for magnet power supplies or controllers for RF systems. The interface definition of the bus was fixed before the SCU design started. This enabled other departments to develop slave cards for this interface.

The decision to use a a 16-bit parallel bus was based mainly on lots of experience with other parallel backplanes (8/16-bit), albeit with lower speeds. Another important design criteria was the possibility to analyze the bus transactions with an external logic analyzer. These were still widely in use when the design process started. In-System debug techniques like SignalTap from Altera or ChipScope from Xilinx where not yet used. This changed with the first prototypes of the SCU and In-System Debugging became a standard. The commissioning of the parallel backplane \succeq turned out to be quite difficult because of electrical interference. It took several versions of the backplane PCB and the addition of active termination to get the parallel bus into working condition. Even then, a few bus signals needed to be deglitched inside of the FPGA, first of all the dedicated interrupt signals.

The serial PCIe connection between the FPGA and the COM Express module was by far easier to build than the parallel backplane PCB. During the prototyping phase we used a modified PCIe card, where the PCIe lanes were rerouted with magnet wire. This enabled us to test the PCIe controller in the Altera FPGA and our PCIe connection worked perfectly in the first pcb version of the SCU. The PCIe controller is electrically based on an Arria transceiver. We used the same transceivers for a GbE connection (synchronous ethernet for timing) with an SFP. This was just as easy to build as the PCIe link.

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The SCU4 will have for the first time a USB connection to the FPGA which provides a UART interface for debugging and an Etherbone connection to the SoC inside the FPGA. It will replace two dedicated UART connectors. The USB interface is already used in timing receivers which use similar architecture and has proven to be reliable. The interface features USB2 and is based on the EZ USB FX2LP from Cypress.

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SECOND USE CASE FOR SCU

It is planned to give the SCU hardware another use case as a timing message generator, called Data Master, for the General Machine Timing (GMT) System. Currently another hardware, based on a PCIe card, is used for this purpose. The SCU hardware has to be designed with this second use case in mind. This does mainly imply the possibility to be able to use a bigger FPGA with more internal memory. The difference will be roughly four times the size of the internal memory of the PCIe card. This will enable the Data Master to handle more and bigger schedules.

CONCLUSION

The maintainability is one of the major issues with electronic systems in 'big science'. With high level of complication and limited manpower, the process of designing and commissioning takes years. Thus, the lifetime should reach decades. On the other hand, continuously altering market of electronic components makes it difficult to produce devices only few years after designing. Keeping projects up to date while maintaining backward compatibility is getting a major challenge.

With its fourth generation, the SCU project can be considered mature. It's proven with already over 500 of running devices and it's free of major problems. On the other hand, using state-of-the-art components in SCU 4 extends the project lifetime by years. This gives a good perspective for retrofitting the old GSI's Unilac control system as well as providing control systems for the newly built facilities of FAIR.

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