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# DESIGN OF RELIABLE CONTROL WITH STAR-TOPOLOGY FIELDBUS COMMUNICATION FOR AN ELECTRON CYCLOTRON RESONANCE ION SOURCE AT RIBF

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*Abstract*

In the RIKEN Radioactive Isotope Beam Factory (RIBF) project, a superconducting linear accelerator has been implemented to enhance the beam energy necessary for promoting super-heavy element search experiments. A new 28-GHz electron cyclotron resonance ion source (ECRIS) has been installed upstream of it. Its control system has been planned to comprise the Yokogawa FA-M3V series, which is a programmable logic controller (PLC) with Experimental Physics and Industrial Control System (EPICS) because basically the same control system has been successfully operated for our existing ECRIS control system. However, the existing ECRIS control system with PLCs has a disadvantage of low reliability for communications between PLC stations. In addition, higher expandability is required because some devices, such as a power supply for an oven, will be changed depending on ion species produced at the ion source. In the new system, we have designed the control system by utilizing a star-topology fieldbus for communications between the PLC stations to establish safety and expandability.

## INTRODUCTION

The RIKEN Radioactive Isotope Beam Factory (RIBF) accelerator facility consists of five cyclotrons, including a superconducting ring cyclotron, and two linear accelerators [1]. In the RIBF, we constructed a distributed control system based on the Experimental Physics and Industrial Control System (EPICS) for electromagnet power supplies, beam diagnostic instruments, vacuum control systems, etc. [2]. In FY2016, we started a new project at RIKEN RIBF to further advance synthesis of super-heavy elements with atomic numbers greater than 119, and the main points are as follows [3]:

A superconducting linear accelerator (SRILAC) is newly installed in the downstream part of the RIKEN linear accelerator (RILAC) to enhance the beam energy [4]. To increase the beam intensity for RILAC, the existing 18-GHz electron cyclotron resonance ion source (ECRIS) [5] is also upgraded to a new superconducting ECRIS (SC-ECRIS) [6].

Of these two, the new SC-ECRIS has the same structure as the RIKEN 28-GHz SC-ECRIS installed in the upstream of RILAC2 [7], which is one of the other injectors of the RIBF currently being operated. Therefore, as the devices to be controlled are almost the same as the RIKEN 28-GHz SC-ECRIS, the new SC-ECRIS control system should be constructed based on the current RIKEN 28-GHz SC-ECRIS control system with several improvements to overcome the limitations of the present system. In this proceeding, we discuss disadvantages of the current RIKEN 28-GHz ECRIS control system and report the design of the newly constructed control system in detail.

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## RIKEN 28-GHZ SC-ECRIS CONTROL SYSTEM

### *System Concept*

As the main feature of the RIKEN 28-GHz SC-ECRIS control system, Programmable Logic Controllers (PLCs) of the Yokogawa FA-M3 series and EPICS are utilized. The detailed system chart is shown in Fig. 1. The control system is mainly divided into two parts. One is F3RP61-2L, which is a CPU running Linux, to provide the operation services such as controlling of gas valves and power supplies [8]. In the case of the F3RP61-2L-based PLC station, EPICS is installed on the Linux-running system as the PLC CPU's operating system and the EPICS Input/Output Controller (IOC) is implemented as the middle layer for operation services, the so-called embedded EPICS. The other is the part of the implementation of the interlock function as a safety system [9]. Because the sequence CPU-based PLC station has the real-time feature, it is suitable for constructing the safety system, in which not so fast response, such as less than 1 ms, is required. Therefore, the interlock function is realized by the sequence CPU-based PLC station independently from the Linux-CPU-based PLC station, and the state of interlock is monitored by another external EPICS IOC via the TCP/IP network.

As the interlock, the system realizes the function of safely turning off the high-voltage power supply at the time of door opening, turning off the radio frequency (RF) at the time of vacuum abnormality.

### *Communication between PLC Stations*

In the RIKEN 28-GHz SC-ECRIS control system, the main station, which is the installed Linux PLC CPU, manages four substations connected by fieldbus communication electrically isolated by optical fibers. In the case of the Yokogawa FA-M3 series, the fieldbus is called the FA bus. They communicate through FA-bus modules. Because heavy ions generated by an ion source are extracted to the low-energy beam transport by high voltage,

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substations also need to be implemented at the high-voltage stage in some cases. As a typical example, the power supplies for the high-temperature oven method [10] and BIAS disk method [11] need to install the PLC substation on the high-voltage stage. Therefore, the optical fiber, being an insulator, is adopted for fieldbus communication between the main station and the substations. Consequently, the signal exchange between the sequence PLC CPU-based station for interlock and the Linux CPU-based PLC station needs to use EPICS Channel Access (CA) via the TCP/IP network or electrical signal.

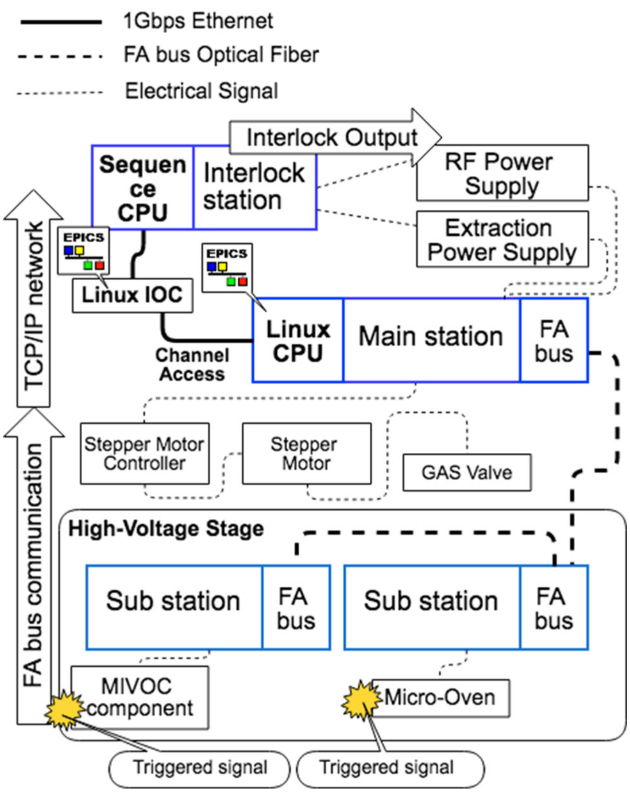


Figure 1: System chart of RIKEN 28-GHz SC-ECRIS control system. CA protocol is utilized for operation services and triggered signal.

## *Reliability of TCP/IP-based Interlock*

There are two methods for sending the interlock signal from the Linux CPU PLC station to the sequence CPU PLC station, viz., sending an electrical signal to the sequence CPU PLC station via the Linux PLC's output module and sending the interlock signal by EPICS CA via TCP/IP. When using state information of the substation implemented in the high-voltage stage as an interlock signal, this system has the means to exchange signals only by the EPICS CA via the TCP/IP network. In general, the reliability of the CA-based interlock system is not high because of the failure of the network switch in the network route, the problem of slow signal transmission speed compared with the bus access, and the problem of reliability of the EPICS IOC. Thereby, the reliability of the signal through TCP/IP is lower than that of the electric signal, and thus the reliability of the interlock is also not relatively high.

# NEW SC-ECRIS CONTROL SYSTEM

## *System Design*

In the new project, a new SC-ECRIS is installed upstream of RILAC to increase the beam intensity for RILAC. The photograph of the new SC-ECRIS for SRILAC is shown in Fig. 2. Considering the new SC-ECRIS for SRILAC, the control system should follow the current RIKEN 28-GHz SC-ECRIS control system upstream of RILAC2, because the RIKEN 28-GHz SC-ECRIS control system has achieved success in the RIBF project. Thus, in the case of the new SC-ECRIS control system, we have adopted the Yokogawa FA-M3V series, which is the upgraded FA-M3, for system construction. On the other hand, we should also solve the disadvantage of low reliability for interlock features in the RIKEN 28-GHz SC-ECRIS control system when constructing the new SC-ECRIS control system. Accordingly, to solve the disadvantage, a new SC-ECRIS control system has been designed by implementing two different types of CPUs in the main PLC station. Essentially, the sequence PLC CPU in the first slot and the Linux PLC CPU in the second slot have been implemented in the same PLC base module. In the sequence PLC CPU, the ladder program runs for the interlock system, and the Linux CPU runs the EPICS IOC and provides operation services to users via the EPICS CA protocol. Currently, the new SC-ECRIS control system consists of a main PLC station and five PLC sub stations with star-topology fieldbus communication using optical FA bus modules. The detailed system diagram is shown in Fig. 3.

At present, this control system does not include the control of superconducting electromagnet power supplies. Control of superconducting electromagnet power supplies is implemented in a system consisting of another controller and client without EPICS IOC. The system implementation test with EPICS is in progress now.

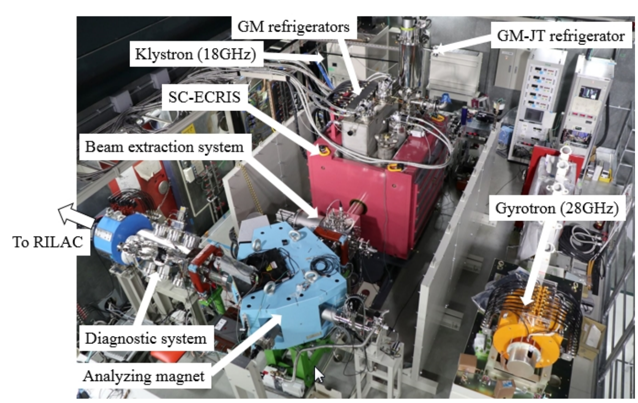


Figure 2: Newly installed SC-ECRIS for SRILAC. Currently, an 18-GHz RF source (Klystron) is only used for the beam commissioning [5].

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### Interlock

Generally, X-rays are generated during the operation of the ion source and the high voltage is utilized for extraction of heavy ions generated. Therefore, this interlock has to prevent workers from exposure to X-ray and/or accidental electrification.

Interlocks are roughly divided into two types. One is a human protection system, which has a mechanism to turn off the RF power and power supplies for high-voltage beam extraction when a person enters the ion source room. This interlock system utilizes the opening of doors and entrance information as the triggers. The other interlock is a machine protection system. The system monitors the cooling water, vacuum condition, etc., and automatically stops the ion source and the devices constituting it, safely in case of abnormality.

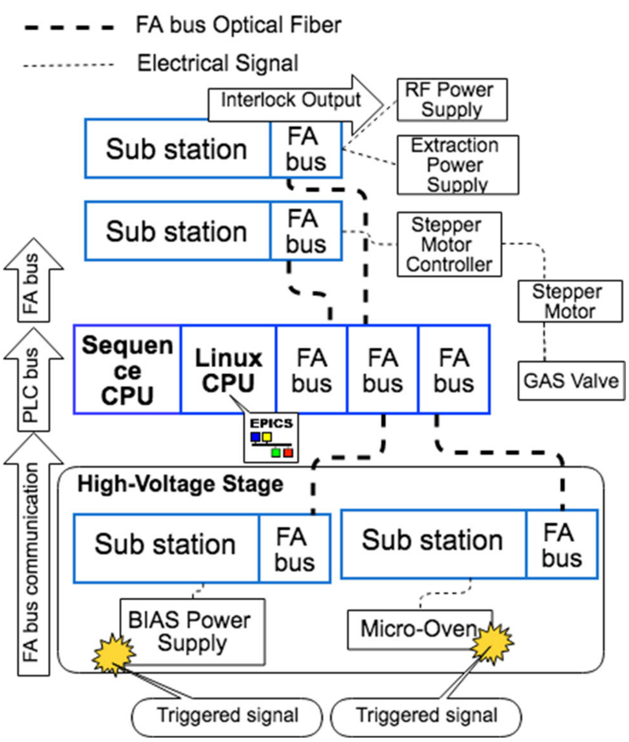


Figure 3: System chart of new SC-ECRIS control system for SRILAC. Interlock signal is delivered by bus communications.

### I/O Sharing Method

The feature of the Yokogawa FA-M3V series is that, as a behavior when there are two CPUs, reading can be done from both CPUs unconditionally, but direct instructions to the output module adopt exclusive control. Therefore, the basic write (output control) is performed only from the sequence PLC CPU, when performing output control from the EPICS IOC on the Linux PLC CPU; it will be realized via internal registers of the sequence PLC CPU, for example, I00001.

### I/O Refresh Time for FA Bus using Optical Fiber

According to Reference [12], the I/O refresh time for each access type (read/write) via the optical FA bus module is estimated to be the product of the access time and "Number of modules converted to a 16-point basis". The access time is the sum of "Time dependent on access type" and "Time dependent on transmission distance". Based on this estimation, the theoretical transfer I/O refresh time is 16.8 μs in this system. This value is sufficiently higher than the TCP/IP-based network speed.

### System Availability

Based on the status information of the doors and entrance, we are able to provide a human safety mechanism as an interlock system of RF source and extraction voltage of SC-ECRIS. Accordingly, it is possible to realize the interlock signal for the machine protection system via FA bus communication without going through the TCP/IP network, even though the control of power supply for the oven system is mounted on the high-voltage stage. As the system behavior, the oven power supply is turned off by triggered by the degree of vacuum and cooling water temperature.

## CONCLUSION

We solved the disadvantage of the insufficient reliability of the interlocks in the RIKEN 28-GHz SC-ECRIS control system and constructed a control system of the new SC-ECRIS for SRILAC. This new SC-ECRIS control system was successfully used in the test operation of the new SC-ECRIS performed in August 2018 without any serious problem. Because of the mounting of two CPUs in one base unit, it is possible to exchange the trigger signal for interlocking with the sequence PLC CPU from the Linux PLC CPU via the FA bus on the PLC base module. Therefore, it is possible to share the interlock signal of the high-voltage stage with the Linux PLC CPU and the sequence PLC CPU without going through the TCP/IP network, and it improves the system reliability of the interlock feature successfully without lowering the conventional system usability.

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