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DEVELOPMENT OF TRIGGERED SCALER TO DETECT MISS-TRIGGER

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Abstract

A "triggered scaler" has been developed for J-PARC accelerators. It is a PLC-type scaler with memory-buffers. Number of pulsed signals is counted and stored in a cell of memory-buffer, then, each external trigger (25 Hz) shifts the pointer to the cell. The buffer size (192) is designed to store one machine-cycle (2480 ms or 5200 ms in J-PARC). Demonstrative measurements using a prototype module are reported. In addition, scheme to detect miss-trigger events are discussed.

INTRODUCTION

J-PARC (Japan Proton Accelerator Research Complex) is a high-intensity proton accelerator complex. It consists of three accelerators: a) 400-MeV Linac (LI), b) 3-GeV Rapid Cycling Synchrotron (RCS), c) 30-GeV Main Ring (MR) [1-2]. Since the initial beam in 2006, beam powers for experimental facilities were steadily increased [3].

There are two time cycles in J-PARC. The rapid cycle, 25 Hz, is used at LI and RCS. The slow cycle is used at MR. In 2018, when MR delivers proton beams to Neutrino Facility (Hadron Facility), 2480 ms (5200 ms) is used, respectively. Typical timing scheme is shown in Fig. 1. Since the slow cycle determines the overall time behaviour of accelerators, it is called “Machine Cycle”.

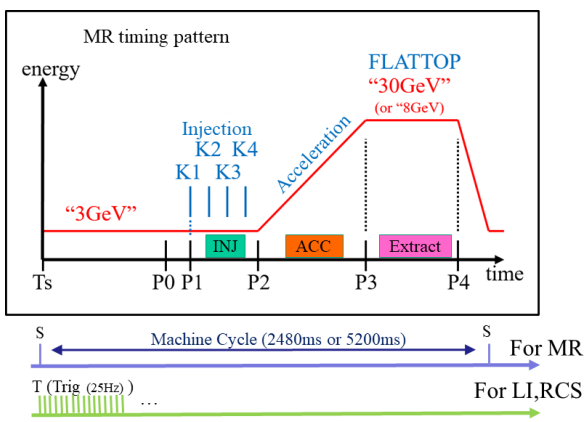

Figure 1: Typical timing scheme of J-PARC accelerators.

TIMING SYSTEM AND MISS-TRIGGERS

Overview of the Timing System

The control system for J-PARC accelerators was developed using the EPICS (Experimental Physics and Industrial Control System) toolkit [4-5]. Addition to it, we have a dedicated timing system [6].

The timing system consists of one send module and several receiver modules. Both modules were developed as home-design VME modules. Event-codes, called “types”, generated by the send module are distributed to receiver modules. A fiber-optic cable network is used for “type” distribution, using several O/E (or E/O) modules. According to the received “type”, each receiver module generates eight independent trigger signals for accelerator components. There are 118/43/45 receiver modules used in LI/RCS/MR, respectively.

Miss-trigger Troubles in J-PARC

During the operation since 2006, we have experienced a few miss-trigger troubles. Here we show three cases.

The first case started as a fault of MR kickers in February, 2014. Soon we found other MR components also miss-behaved occasionally. Finally we found that missing of the 25-Hz trigger-clock occurred in the whole MR area at the rate ~10 times per day at maximum. In May, 2014, we replaced an O/E module, which is located at the root position of MR area.

The second case appeared as a bad quality beam during stable beam delivery to Hadron Facility in November, 2016. Here “bad quality” means that beam size was slightly larger than normal, but still acceptable for experiments. Such beams appeared a few times per month [7]. Some O/E modules were replaced, but not effective. In May, 2017, we found that a receiver module for one of MR steering magnets showed momentary errors, hence, miss-triggers occurred. The timestamps of errors were retrieved from the archive system, which agreed with the timestamps of bad beams. Later survey showed that the errors were caused by external common-mode noises. We added ferrite cores to metal cables connected to the receiver module.

The third case was happen in November to December, 2017. An O/E module, which was used to send the 25-Hz trigger-clock signals from RCS to MR, started to produce fake signals (Fig. 2). Since fake signals affected a critical beam diagnostic system, accelerator operation suspended a few to 10 times in a day. We replaced the O/E module.

In the first and the third cases, it was difficult to find the troublesome module among many suspicious modules. In the second case, miss-trigger events were very rare, and it took six months to find the origin. Such experiences suggested us to develop a new module to detect a miss-trigger.

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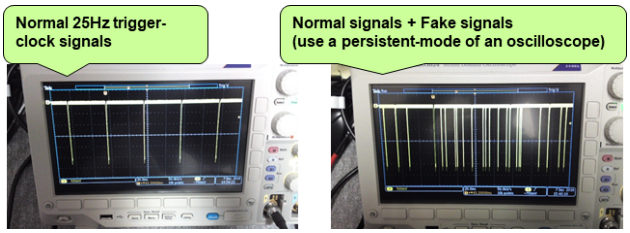

Figure 2: Observed fake signals.

TRIGGERED SCALER

Design of the Module

The conceptual design of the triggered scaler is shown in Fig. 3. Blue part is the module, and external input signals are also shown. The module receives "S" (start of the machine cycle) and "Trig" (start of the rapid cycle, 25 Hz) signals as reference signals, which are generated and distributed by the J-PARC timing system. The module has four input channels, and each of them has dual memory-buffers (16 bit x 192 cells x 2).

In principle, it works as a scaler module. The FPGA logic inside (FPGA_1) writes counts to memory-buffers. When "S" comes, FPGA_1 starts a counting process. It writes a value to the first cell of the first memory-buffer. Each time "Trig" comes, FPGA_1 shifts the pointer to the cell. When next "S" comes, the pointer is moved to the first cell of the second memory-buffer. This scheme allows us to retrieve the counts of input signals during the last machine cycle. In operation with a machine cycle of 2480 ms (5200 ms), 62 (130) of 192 cells are used, respectively. The logic in FPGA_2 reads the memory-buffers, detects a miss-trigger (or verifies no miss-trigger) in them, and sets error flags if necessary.

Development of the triggered scaler was carried out by a company, Hitachi Zosen [8]. By 2016, four prototype pieces were made as Yokogawa PLC-type modules, since it is a standard I/O form in J-PARC MR [9].

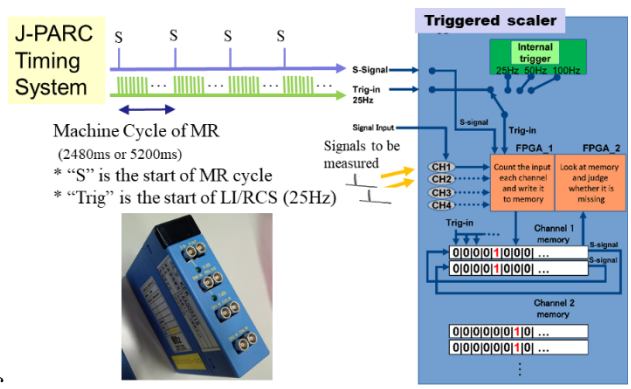

Figure 3: Design of the triggered scaler.

Measurements using a Prototype Module

For the first field test, we prepared a test setup (Fig.4). It consists of a prototype module and a CPU module, where EPICS is running. In January, 2018, we measured a trigger signal for MR injection kickers. In normal operation, there are four successive injections (so-called "K1-K4") in a machine cycle. The observed data showed that four successive "1" values appear in the memory-buffer (Fig. 4).

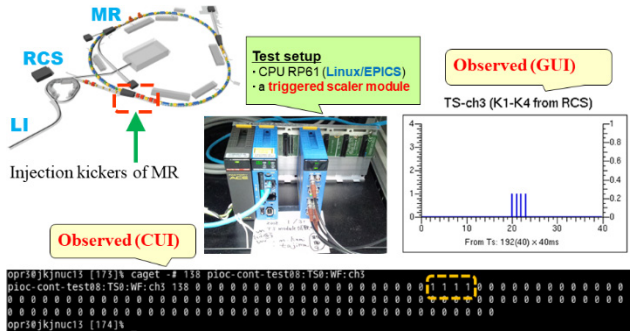

Figure 4: Measurement of a trigger for injection kickers.

As a next demonstration, we measured a RF signal (MR-ring circulation signal), which is generated by an LLRF system. Every machine cycle, 3-GeV protons are injected into MR, then accelerated up to 30-GeV. In Fig. 5, the graph reflects frequency shift of the RF signal, during injection and acceleration periods.

The number of counts in a 40-ms bin were summarized. When beam energy is 3 GeV (8 GeV, 30 GeV), 7429 (7608-7609, 7648) was observed, respectively. Observed counts agree well with the RF parameters (Fig. 6).

Measurements above show that a triggered scaler works as we expected. It is worth noting that a triggered scaler can be a tool to visualize various trigger signals.

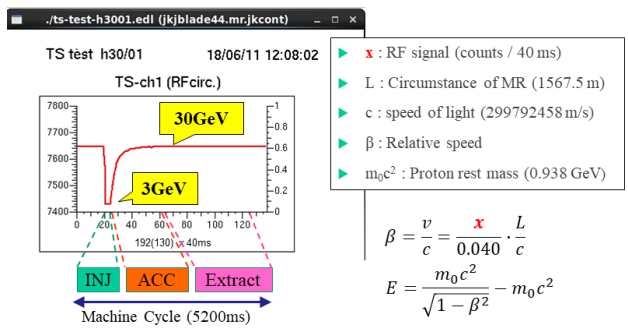

Figure 5: Measurement of a RF signal.

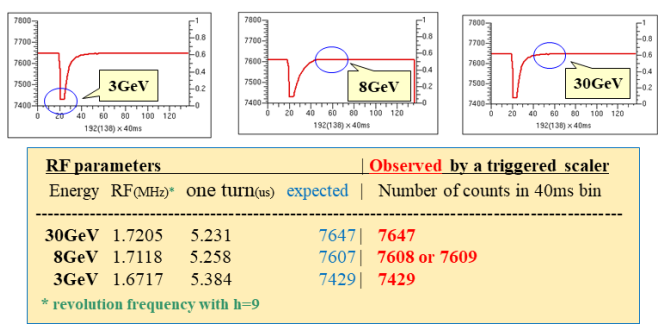

Figure 6: Numbers of counts in 40-ms bin observed at the three different energies.

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TO DETECT MISS-TRIGGERS

Three Cases of Miss-triggers

Based on our experiences, there cases of miss-trigger events are considered. Here let us consider the injection kicker signal (K1-K4) as an input signal. The normal view of K1-K4 signal is shown as the reference in Fig. 4. The first case, "miss trigger", is that one trigger (or more) disappears. The second case, "irregular trigger", is that unexpected triggers are overlapped into the original K1-K4 signal. The third one, "double trigger", is that one trigger (or more) is counted double. This could occur when a cable termination is incorrect. Three types of miss-trigger events are shown in Fig. 7.

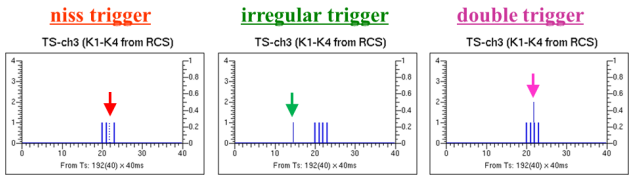

Figure 7: Three cases of miss-trigger events.

EPICS Databases for Triggered Scaler

For easier handling, registers and memory-buffers of the module (hardware layer) were defined in EPICS databases. Part of definitions are given in Fig. 8.

We are developing two more layers: over the hardware layer, (a) operation layers, which describe specific parts for rapid-cycle and for slow-cycle, and over the operation layer, (b) application layers, which correspond to various applications (K1-K4 observation, surveillance of RF signals, miss-trigger detection, etc.). Details are given elsewhere [10].

PV name	Data type	Reg. Address	Description
pageNow	longin	9	Page number, 0 or 1, which point to the active memory buffer
triggerNow	longin	10	Position of a memory buffer, 0 to 191, where a counter value is written
pageSet	longout	11	Switch a page number, 0 or 1, which memory buffer to be read from CPU
errStatus	longin	14	Error status in counting process
triggerInCycle	longin	16	Number of triggers in the previous S-signal period
wf:ch1~ch4	waveform	33-224 289-480 545-736 801-992	Array data of memory buffer (192) for ch1~ch4

Figure 8: Hardware layer definitions of triggered scaler.

Software to Detect Miss-triggers

In stable beam-delivery operations, a miss trigger can occur as a momentary event. There are two issues what we have to discuss.

The first issue is methods to detect a miss-trigger event. For a rapid-cycle mode, an embedded logic in the FPGA_2, which detects a non-zero value in a cell, would be used. For a slow-cycle mode, comparing the latest memory-buffer with a reference is essential. For the latter mode, it often required machine parameters to judge whether a miss-trigger event occurs or not. Thus, combination of EPICS databases and sequencers would be used.

The second issue is what we have to do after a miss-trigger is detected. Studies of routines to save related parameters (shot-number, DCCT waveform, etc.) are in progress.

CONCLUSION

The "triggered scaler" has been developed for J-PARC accelerators. It is a customized module of Yokogawa-type PLC. A prototype module was used to measure accelerator signals, and showed expected functionalities.

Software to detect three cases of miss-triggers is discussed. EPICS databases to access module hardware were developed. Routines to detect miss-trigger events are in progress.

We appreciate the RF team of J-PARC MR, especially Yasuyuki Sugiyama and Keigo Hara, for their helps during test measurements using RF signals. We also thank all accelerator members and companies for their efforts to maintain the control system.

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