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OPERATIONAL EXPERIENCE OF THE DIGITAL LLRF CONTROL SYSTEM AT THE BOOSTER RING OF TAIWAN PHOTON SOURCE

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Abstract

The purpose of a Low-Level Radio Frequency (LLRF) system is to control the accelerating cavity field amplitude and phase. To have better RF field stability, precise control and high noise reduction, a digital LLRF control system based on Field Programmable Gate Arrays (FPGA) was developed at NSRRC. We replaced the analog LLRF system with a digital version for the TPS booster ring at the beginning of 2018. During routine operation of the booster RF, some faults occurred when the digital LLRF operated in the energy savings mode. The performance and operational experience of the digital LLRF for the TPS booster will be presented here.

INTRODUCTION

The Taiwan Photon Source (TPS) at the NSRRC is a third-generation light source operating at 3 GeV. The field in the accelerating cavity is controlled by a Low-Level Radio Frequency (LLRF) system. A digital LLRF (DLLRF) control system based on Field Programmable Gate Arrays (FPGA) is expected to exhibit improved RF field stability, precise control and high noise reduction. The analog LLRF system for the TPS booster ring was replaced by a digital version at the beginning of 2018 [1]. Since the digital tuner loop is not implemented yet, we only replaced the modules in the RF path for the digital system to keep the tuner function and the interlock protection system. The Programmable Logic Controller (PLC), including the analog tuner loop and the function of interlock protection, is still contained in the DLLRF system. Figure 1 shows the architecture and photos of the TPS booster DLLRF system.

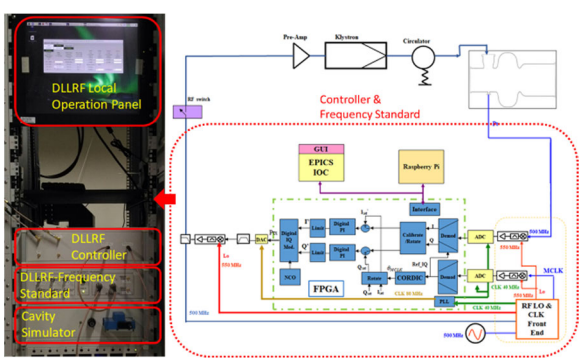

Figure 1: Architecture and photos of the TPS booster DLLRF system.

During full power routine operation with the DLLRF system, the difference between set points and measured values can be controlled to 0.32 ± 0.52 % and 0.01 ± 0.13 degrees for the cavity voltage amplitude and phase, respectively. The sidebands of the 60 Hz noise and its harmonics can be suppressed down to -70 dBc. The details of the design and implementation of the DLLRF controller, the hardware architecture, test results and operation performance of the TPS booster DLLRF system can be found in [1-3].

The operational status can be monitored by the data acquisition system, including the transient data recorder for trip analysis and the archiver for the slow long-term data recorder. Figure 2 shows the hardware structure for the TPS booster RF data acquisition system. All the analog signals are collected on the junction box and distributed to the digitizers. Signal buffers are placed between junction box and digitizers to avoid any impedance mismatch. Four digitizers are used for the EPICS IOC to collect historic data at a slow sampling rate (about 1 kHz) and one digitizer is used for the transient recorder with a sampling rate of up to 250 kHz.

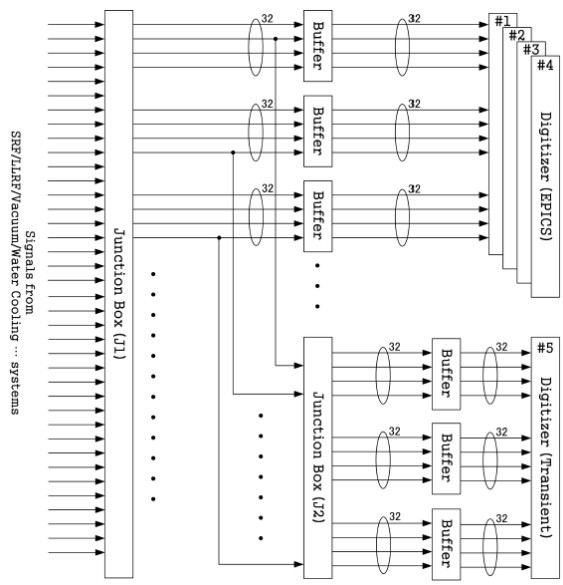

Figure 2: Hardware structure of the data acquisition system.

A function to save energy [4] is implemented in the TPS booster DLLRF by controlling the klystron cathode current and cavity voltage following the injection timing signal [5]. During routine operation, some faults occurred when the DLLRF operated in the energy saving mode. The operational experience of the DLLRF for the TPS booster as well as trip analyses are reported in the following sections.

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OPERATION STATUS

The DLLRF system for the TPS booster was installed on Feburary 2018 and was found to be stable without the function of energy saving. However, when the function of energy saving was turned on, the DLLRF system tripped. The related signals are shown in Fig. 3 for the transient data. The cavity gap voltage was close to saturation at the start of energy ramping. This is due to an unstable oscillation of the cavity gap voltage during the beginning of full klystron power operation. The LLRF status on the PLC would turn to tune mode when the oscillating cavity gap voltage reached its lower limit, and the DLLRF would cut-off the RF forward power due to an inconsistent status.

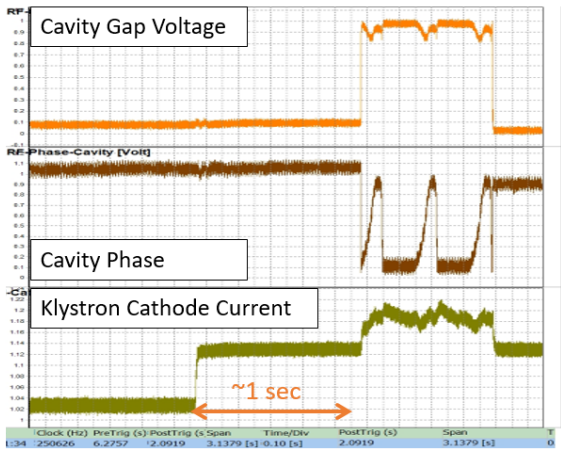

Figure 3: Related signals during the trip event. The y-axis displays the raw reading values in Volt.

This oscillation is due to the phase shift of the RF loop resulting from a changing klystron cathode current, as shown in Fig. 4. The cavity phase shifts by about 60° while the klystron adjusts to full power operation, and back again to 0° after about 6 sec. The PI gain of the digital LLRF controller was optimized for full power operation and not for a phase shift in the loop. After adjusting the PI gain, the TPS booster RF operates stable with the DLLRF system in the energy savings mode. Historical data for stable operation with energy saving are shown in Fig. 5.

Figure 4: Measurement of related signals in tune mode.

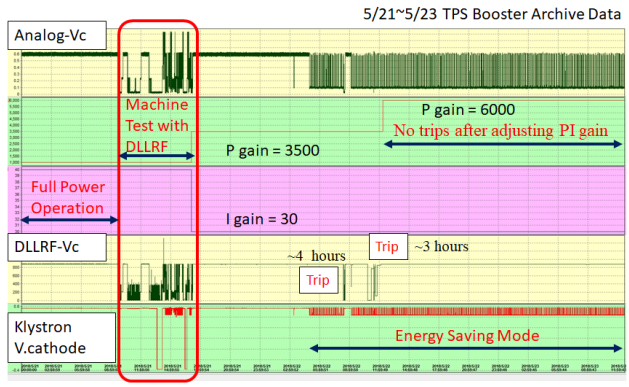

Figure 5: Historical data for stable operation with energy saving. After adjusting the PI gain, no trips occur during energy savings operation.

PI OPTIMIZATION

A simple LLRF system model was developed to optimize the PI gain offline. This simulation program was developed with MATLAB and Fig. 6 shows its block diagram.

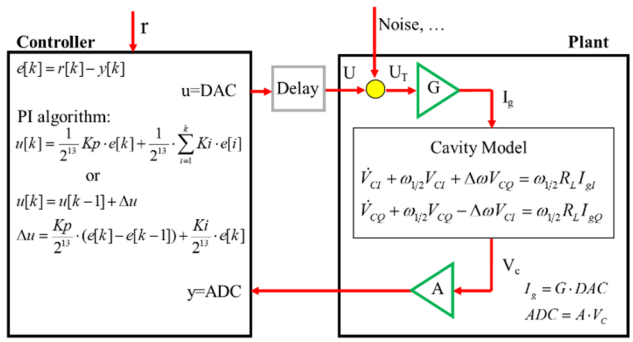

Figure 6: Block diagram of a LLRF system simulation model.

The RF plant model includes the cavity response and the calibration of the DAC to generator current and the cavity voltage to ADC. The equations of the cavity model can be written as follows [6]:

$$\dot{V}_{CI} + \omega_{1/2} V_{CI} + \Delta\omega V_{CQ} = \omega_{1/2} R_L I_{gI}$$
$$\dot{V}_{CQ} + \omega_{1/2} V_{CI} - \Delta\omega V_{CI} = \omega_{1/2} R_L I_{gI} \quad (1)$$

where $\omega_{1/2} = \omega_{cav}/2Q_L$ and $\Delta\omega = \omega_{cav} - \omega_{RF}$ and the calibration coefficients G and A for $I_g = \mathrm{G} \cdot \mathrm{DAC}$ and $\mathrm{ADC} = \mathrm{A} \cdot V_C$ are obtained from measurements. The controller model describes the function of the PI algorithm in the DLLRF controller. For the present design, we use the theoretical form including a 13-bit truncation in the digital implementation, which can be defined as follows:

$$e[k] = r[k] - y[k] \quad (2)$$

$$u[k] = \frac{1}{2^{13}} Kp \cdot e[k] + \frac{1}{2^{13}} \cdot \sum_{i=1}^{k} Ki \cdot e[i] \quad (3)$$

For the older design we use the difference equation algorithm, which is:

$$u[k] = u[k-1] + \frac{Kp}{2^{13}} \cdot (e[k] - e[k-1]) + \frac{Ki}{2^{13}} \cdot e[k] \quad (4)$$

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However, errors coming from the 13-bit truncation of the proportional term accumulate in eq. (4) resulting in a poor performance comparison with eq. (3), as shown in Table 1.

Table 1: Analysis of the input signal with different PI algorithms

	Eq. (3)	Eq. (4)
Amplitude SP	905.3 kV	905.3 kV
Amplitude mean	905.09	898.23
Amplitude RMS	± 0.12 %	± 0.19 %
Phase SP	12.1°	12.1°
Phase mean	11.95 °	10.29 °
Phase RMS	± 0.20 °	± 0.21 °

Figure 7 shows the cavity gap voltage signals while the feed forward table was turned on. An additional pulse waveform is added into the RF output. The response of the cavity gap voltage is different with different PI gains and delay time. Therefore, the delay time of the whole RF system can be determined by fitting these waveform signals. The simulation and the measurements are consistent with each other for the 3 μsec delay. The simulation predicts instability for some PI gain values with a 60° loop phase shift, as shown in Fig. 8. This instability is consistent with observation.

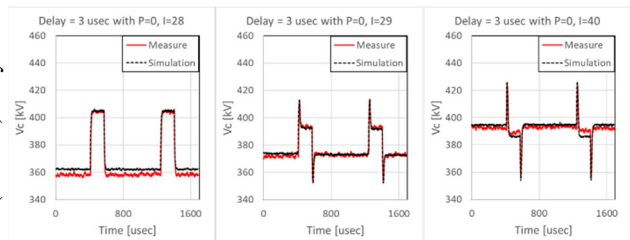

Figure 7: Cavity gap voltage with the feed forward table turned on for different I gain.

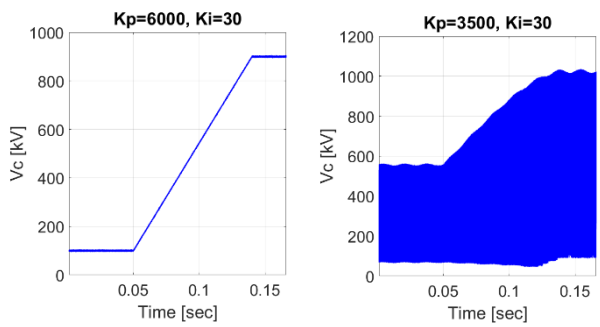

Figure 8: Simulation results for the cavity voltage during ramping with different PI gains. A small P gain may cause the instability.

Figure 9 shows the stable region for PI gains with a 60° loop phase shift obtained from the simulation. The optimized gain is determined by minimizing the RMS errors during ramping in the stable region. The finial gains are set to 7500 and 24 for P and I, respectively. The difference between set points and measured values during ramping with the energy saving function and optimized PI gains can be controlled within 0.05 ± 0.28 % and 0.14 ± 0.21 degrees for the cavity voltage amplitude and phase, respectively. With tuned PI gains, the TPS booster digital LLRF system operates stable with active energy savings function.

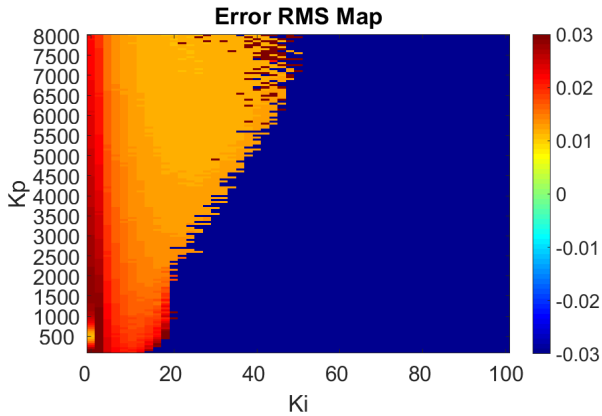

Figure 9: The map of RMS values for the errors between set points and measurements. Negative values indicate an unstable region.

CONCLUSION

The analog LLRF system for the TPS booster ring was replaced by a DLLRF system in February 2018. A function to save energy by controlling the klystron cathode current and cavity voltage with the injection signal, is implemented as well. It may cause instability due to the phase shift in the RF loop resulting from the change of the klystron cathode current. The PI gains need to be re-optimized for the energy savings mode to obtain stable operation. A simple LLRF system model was developed to optimize the PI gains offline. The instability predicted by the simulation is consistent with observations and the optimized PI gains are set to 7500 and 24 for P and I, respectively.

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