ISBN: 978-3-95450-200-4 doi:10.18429/JACoW-PCaPAC2018-THP14

DEVELOPMENT of the NEW SPILL CONTROL DEVICE for J-PARC MR*

T. Kimura†, J-PARC-Center, KEK, Tokami-mura, Ibaraki, Japan

Abstract

J-PARC Main Ring (MR) is there are two operation modes of the fast extraction (FX) and slow extraction (SX) [1,2]. The SX operation used the spill control system. It consists of two kinds of Extraction Quadrupole Magnet (EQ), Ripple Quadrupole Magnet (RQ) and Spill Control Device with Digital Signal Processor (DSP) which calculates and controls it the optimal current pattern using the monitor signal of an extraction beam. It is used to make flatten the extraction beam structure and reduce the ripple noise. The present Spill Control Device needs to be reviewed from the aspect of service life etc. In this presentation, we will focus on improving the versatility of the device and the operability of the DSP program, and explain the development of the next-generation spill control device.

INTRODUCTION

The SX of the J-PARC MR utilizes third integer resonance at Qx = 22.333 [3]. After acceleration of MR, the beam is extracted slowly by betatron tune ramping of main quadrupole magnets in the flattop period of about two seconds. By constant tune ramping speed, the spill structure of slow extraction beam is like Gaussian shape. In physics experiment, the trigger rate or the counting rate of data acquisition system is limited by the hardware and software architecture. In some cases, the detectors cannot separate multiple events, due to collisions with too many particles and the target. In other cases, the data acquisition efficiency can be bad, due to a large dead time when too much beam is extracted. Therefore, the spill beam should be flat and stable sufficiently in extraction period. In order to make flat spill structure, we control the horizontal betatron tune by using the EQ magnets via spill control system. On the other hand, the ripples of main magnet power supply affect to spill structure by spike noise. We reject the ripple noise by RQ magnet.

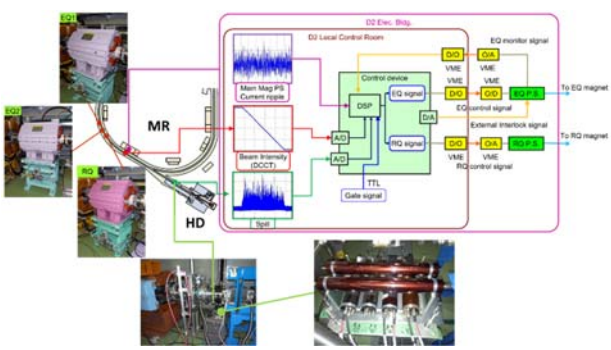

Figure 1: Signal flow of the spill control system.

† kimurata@post.j-parc.jp

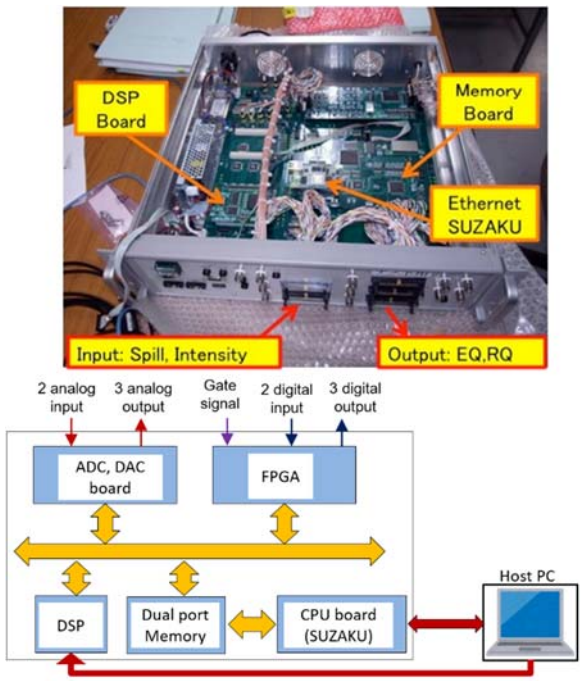

Figure 2: Spill control unit and signal flow.

SPILL CONTROL SYSTEM

Figure 1 shows the signal flow of the spill control system. The spill control unit provides control patterns to EQ and RQ power supply (PS). It is composed of circuit board for DSP, five analog/digital signal inputs, six analog/digital outputs interfaces and RS232 base serial communication interface. The circuit board consists of DSP card, dual port memories and FPGAs. Figure 2 shows the DSP spill control unit and signal flow. The DSP is in charge of spill control calculation. Dual port memory is used to connect the DSP and FPGA, and to share and read spill control calculation data. Table 1 shows the spill control unit spec. The analog input signals consist of control timing gate, residual beam intensity from DCCT and spill intensity of extracted beam from spill monitor.

Table 1: Spill Control Unit Spec

DSP board	TMS320C6713 (TEXAS INSTRUMENTS
ADC, DAC board	C6713DSK (TEXAS INSTRUMENTS)
Sampling frequency	100kHz
Analog Input/Output	±1V, 10kΩ
Digtal Input/Output	LVTTL3.3V, 32bit Positive logic

ISBN: 978-3-95450-200-4 doi:10.18429/JACoW-PCaPAC2018-THP14

The digital input signals consist of EQ PS current signal for verifying control operation and Current ripple data of all main magnet PS for ripple canceller. The analog output signals consist of control value of EQ PS current for monitoring, control value of RQ PS voltage for monitoring and external interlock for stopping EQ PS. The digital output signals consist of EQ PS current control signal, RQ PS voltage control signal and EQ PS current control signal for Dynamic Bump system.

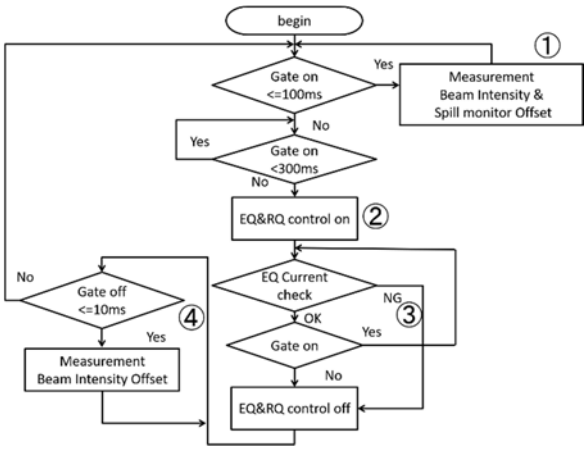

Figure 3: Spill control program flow.

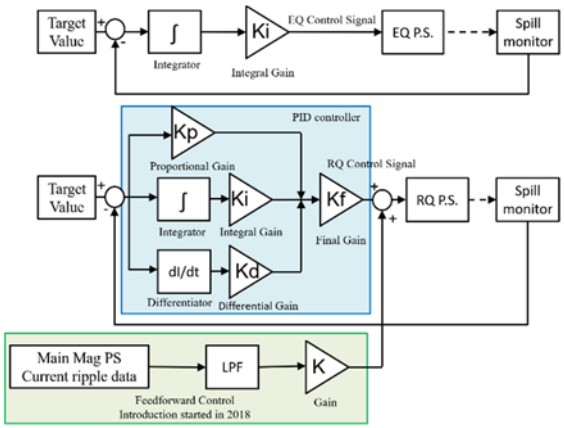

Figure 4: Block diagram of the spill control.

SPILL CONTROL ALGORITHM

Figure 3 shows the spill control program flow. Firstly, when the gate signal on, calculate circulating beam intensity before extraction and spill monitor offset in 100 milliseconds. Also, the target spill height to be controlled so that the beam is extracted in 2 seconds from these data is determined. Secondly, control of EQ and RQ PS is started 300 milliseconds after gate on, and beam extraction is performed. Figure 4 shows the block diagram of the spill control for EQ and RQ PS. Control of EQ makes flat spill structure by using integral control. Control of RQ reduce high frequency ripple noise by using PID control. In 2018, we started a test to cancel the ripple noise by feedforward control by inputting the current ripple data of the main magnet PS. Thirdly, when the gate off, measure the beam intensity offset in 10 milliseconds and prepare for the next beam extraction. Finally, when the EQ PS is being controlled, if the current control value and the output current readback value do not match, control of EQ and RQ PS is stopped. This is a countermeasure the malfunction of the EQ power supply that occurred in 2013. Figure 5 shows beam intensity, EQ current, RQ current, and spill at each timing.

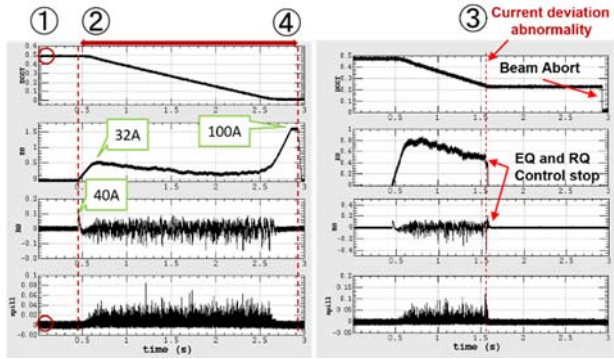

Figure 5: Spill control results.

NEW SPILL CONTROL SYSTEM

Ten years have passed since the development of the present spill control unit. Also, all prepared input/output interfaces including spares are in use, input/output cannot be added even when necessary., Therefore, we need to develop or select a new spill control unit. We selected DSP called SEAGULL made by MTT Corporation as a new spill control unit. Figure 6 shows the new spill control unit.

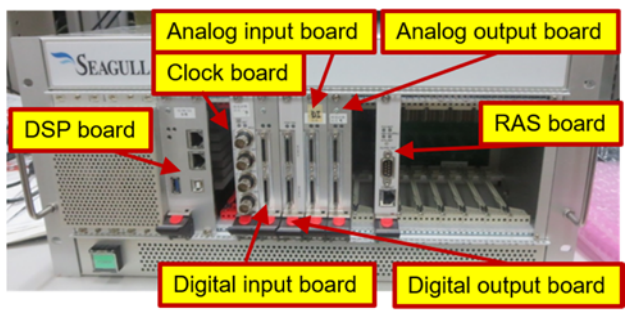

Figure 6: New Spill control unit.

It is composed of DSP board, clock board, RAS (Reliability, Availability, Serviceability) board and each input/output board. Table 2 shows the specifications of each board of the new spill control unit. Each board and the DSP board perform data communication using PCIe DMA transfer. Since each board is modularized, it is easy to add it when input/output needs to be added in the future. Also, we plan to rebuild the spill control system when updating the spill control unit. In the present spill control unit, we can write control program, change control parameters, monitor control state using only dedicated PC. In the new spill control unit, we only perform maintenance, such as changing control programs, on a dedicated PC.

ISBN: 978-3-95450-200-4 doi:10.18429/JACoW-PCaPAC2018-THP14

Table 2: Specification of the New Spill Control Unit

Backplane	PCI Express Gen2
DSP board	KeyStone□ 66AK2H06AAAW24 (TEXAS INSTRUMENTS) ARM Core 1.4GHz×2 DSP Core 1.2GHz×4
Clock board	System Clock ~16MHz
Sampling Frequency	100kHz
Analog Input/Output	32ch 16bit ±10V, 100kΩ
Digtal Input/Output	LVTTL3.3V, 32bit Positive logic

We will make improvements to change control parameters and monitor control status via EPICS IOC from general EPICS client. Figure 7 shows Network of the New Spill control system.

CONCLUSION

The present spill control system introduced in 2009 has contributed to improving the quality of slow extraction beam. However, it took ten years from the development and new development became necessary. In consideration of future input/output scalability, a module type DSP was selected. We would like to develop it aiming for operation from 2019.

REFERENCES

[1] K. Hasegawa *et al.*, "Performance and Status of the J-PARC Accelerators", *Proc. of IPAC 2017*, Copenhagen, Denmark, May 14-19, 2017, pp. 2290-2293.

[2] S. Igarashi *et al.*, "Accelerator Based Neutrino Experiments T2K J-PARC", *Proc. of 13rd Annual Meeting of Particle Accelerator Society of Japan*, Chiba, Aug. 8-10, 2016, pp. 14-18.

[3] M. Tomizawa *et al.*, "Present status and future plans of J-PARC slow extraction", *Proceedings of the 13th Annual Meeting of Particle Accelerator Society of Japan*, Chiba, Japan, Aug. 1-3, 2016, pp. 70-74.

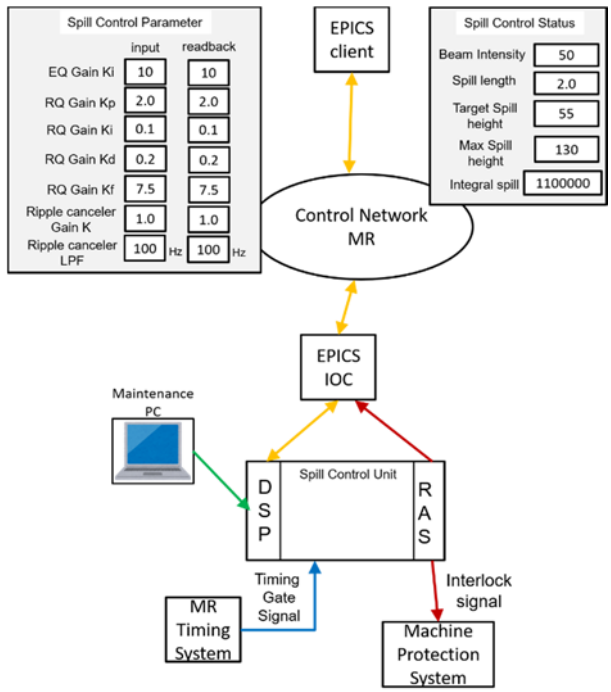

Figure 7: Network of the New Spill control system.