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DEVELOPMENT OF MicroTCA-BASED LOW-LEVEL RADIO FREQUENCY CONTROL SYSTEMS FOR CERL AND STF

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Abstract

Low-level radio frequency (LLRF) control systems based on μTCA standard have been developed for facilities such as compact energy recovery linac (cERL) and superconducting test facility (STF) at the High Energy Accelerator Research Organization (KEK), Japan. Three different types of boards were developed according to their different applications. Experimental physics and industrial control system (EPICS) was selected as the data communication system for all of these μTCA boards. The LLRF systems showed good performance during the beam commissioning. This paper presents the current status of the μTCA-based LLRF systems in the cERL and STF.

INTRODUCTION

The compact energy recovery linac (cERL) and the superconducting test facility (STF) are test facilities for the 3-GeV ERL and international linear collider (ILC), respectively, constructed at the High Energy Accelerator Research Organization (KEK), Japan [1, 2]. The cERL is a 1.3-GHz superconducting radio frequency (SCRF) machine that is operated in the continuous-wave mode. The STF (and ILC) is also a 1.3-GHz SCRF facility but it is operated in the pulse mode. In order to fulfil the desired beam quality requirements, the radio frequency (RF) field in the RF cavity of each accelerator needs to be controlled precisely. For cERL, the amplitude fluctuation of the RF field should be maintained at less than 0.1% (rms) and the phase fluctuation at 0.1° (rms). The STF (or the ILC) requires RF stabilities of 0.07% (RMS) and 0.35° (RMS) with regard to the amplitude and phase, respectively. Field-programmable gate array (FPGA)-based digital low level radio frequency (LLRF) feedback (FB) systems have been applied to stabilize the RF field [3]. The digital platform for the LLRF systems was realized based on the micro telecom computing architecture (μTCA) standard. We have developed three types of μTCA board according to their applications.

In this paper, we first introduce the digital LLRF system, and then we present the various μTCA boards applied in the cERL and STF. Finally, we present the performance of the μTCA-based digital LLRF systems during beam commissioning.

LLRF SYSTEM

Figure 1 shows the block diagram of a typical LLRF system [3]. The RF pick-up signals from all the cavities are down-converted to intermediate frequency (IF) signals. The IF signals are sampled in the next stage and fed to a μTCA FPGA to execute the DSP algorithms. The baseband in the phase and quadrature components (I/Q) are extracted from the IF signal by digital IQ detection algorithm. The I/Q signals are fed to a rotation matrix to compensate the loop phase. The vector-sum signal is then obtained by calculating the superposition of all the cavity pick-up signals. After being filtered by digital low-pass filters, the I/Q components are compared with the set-values and the I/Q errors are calculated. Then, the I/Q errors are regulated by a proportional and integral (PI) FB controller. The regulated I/Q signals are added to the feedforward (FF) models. The combined signals are fed to the I/Q modulator by a digital to analog converter (DAC) to modulate the RF signal from the master oscillator. Finally, the LLRF FB loop is closed by means of a high-power source, which drives the cavities.

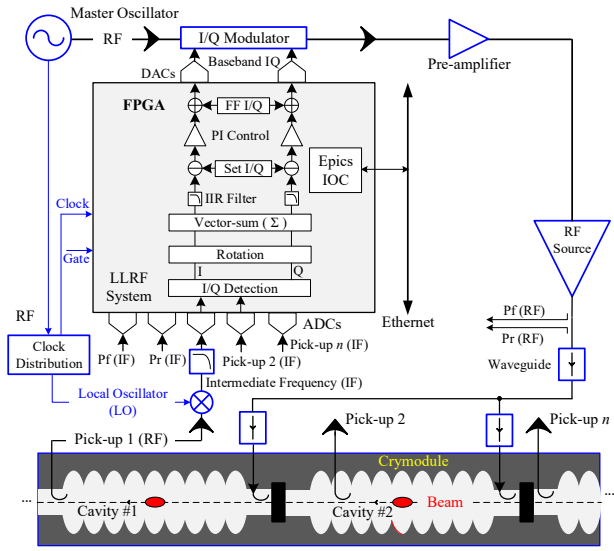

Figure 1: Block diagram of the LLRF system.

μTCA FPGA BOARD

The μTCA FPGA board is the key component of the LLRF system. As shown in Fig. 2, the board integrates ADCs, DACs, an FPGA embedded with power PC (PPC), a digital I/O, and an external trigger. The cavity pick-up signal, forward signal (Pf), reflected signal (Pr), and the reference signal are sampled by the ADCs and fed to the FPGA. The DSP algorithms for the LLRF FB control (see Fig. 1) are implemented in the FPGA. A Linux operation system is installed in the PPC (or ARM). Experimental physics and industrial control system (EPICS) is adopted as the communication protocol. The detailed information about this μTCA board can be found in [4].

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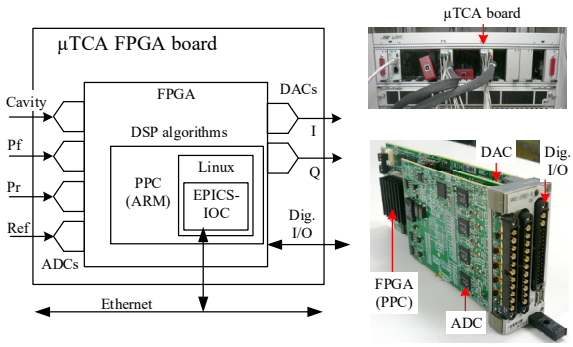

Figure 2: µTCA digital board (type I).

Three types of µTCA boards were developed for the cERL and STF [5]. The µTCA.0 standard type I board and µTCA.4 standard type II boards are mainly used for the LLRF control systems in the cERL and STF, respectively. The main difference between the type I and type II boards is the number of ADCs. We adopted individual cavity control in the cERL (except for the second and third cavities in the injector); therefore, four ADC channels were adequate for our LLRF system. In the STF, we adopted vector-sum control (the vector-sum voltages of the eight cavities were controlled by one controller, see Fig. 1), and accordingly more ADCs were required in the board. The type III board was mainly used for the RF monitor (thus, the DAC is not necessary). The RF signals were directly detected on the board by direct-sampling algorithm without down-conversion (see Fig. 7). The board was equipped with two fast ADCs with sampling frequency up to 400 MSPS [2]. The detailed specifications of these three types of µTCA boards are listed in Table 1 [5].

Table 1: Specifications of the µTCA Boards

TYPE	TYPE I	TYPE II	TYPE III
Facilities	cERL	STF-II	ERL & STF
Function	LLRF	LLRF	Monitor
Standard	µTCA.0	µTCA.4	µTCA.0
ADC	4×16 bits (LTC2208, 130 MSPS)	14×16 bits (AD9650, 105 MSPS)	2×14 bits (ADS5474, 400 MSPS)
FPGA	Virtex-5 FX	Virtex-5 FX	Zynq-700
DAC	4×16 bits (AD9783, 500 MSPS)	2×16 bits (AD9783, 500 MSPS)	N/A
CPU	PPC 440	ARM	PPC 440
OS	Wind River Linux	Xilinx Linux	Wind River Linux

PERFORMANCE

To evaluate the performance of the µTCA LLRF systems of the cERL and STF, the RF field fluctuations were measured by the I/Q detector on the FPGA at the first stage. The achieved field stabilities should be further confirmed by measuring the beam energy fluctuations..

cERL

In the cERL, three two-cell SC cavities were installed in the injector, and two nine-cell SC cavities were installed in the main linac [3]. The beam was accelerated on the crest (i.e., the beam phase φ_b was 0). The measured RF field for the amplitude (left) and phase (right) of the injector and the main linac are illustrated in Fig. 3. Table 2 shows the measured RF stabilities in terms of the different cavities. It should be mentioned that 100-kHz bandwidth digital filters were applied to remove the high-frequency clock jitters.

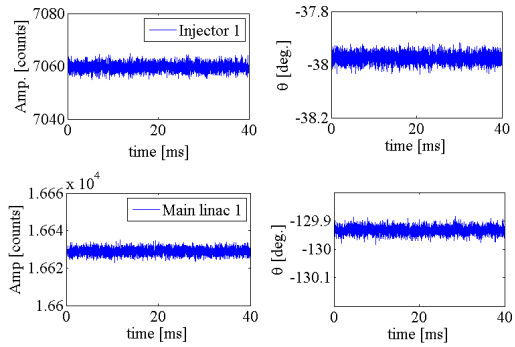

Figure 3: Field stabilities of SC cavities in the injector (top) and main linac (bottom) measured by the µTCA.0 board (type I).

Table 2: RF Stabilities of cERL

Cavity	φ_b	ΔA/A [rms]	Δθ [rms]
Injector 1	0°	0.02%	0.02°
Injectors 2&3	0°	0.02%	0.015°
Main linac 1	0°	0.01%	0.01°
Main linac 2	0°	0.01%	0.01°

To measure the stability of the beam energy, a screen monitor was installed downstream of the bending magnet with a 2.2-m dispersion and a 62.6-µm/pixel resolution. The beam momentum jitter was then calculated by extracting the information of the beam projection on the screen monitor. As shown in Fig. 4, the calibrated beam stability during the measured period of 20 min was approximately 0.0065%.

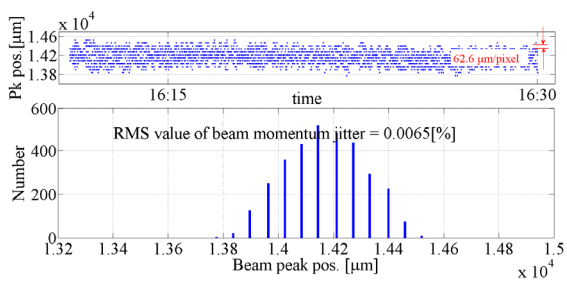

Figure 4: Beam momentum jitter (20 min).

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STF

The injector of the STF consists of a photo-cathode RF-gun and two SC nine-cell cavities in a capture cryomodule. In the main linac, 12 SC nine-cell cavities were installed within two cryomodules driven by a 10-MW multi-beam klystron; however, four cavities suffered from degradation because of heavy field emission. Therefore, only eight cavities were operated in the current status [2]. The beam commissioning of the STF will be performed in the year 2019.

The cavities in the STF (and ILC) were operated in the pulse mode with 1.65-ms pulse duration and 5-Hz repetition rate. Figure 5 illustrates the cavity signals measured by the μTCA.4 board (type II) on the first cryomodule of the main linac. Our target was to maintain a stable vector-sum cavity voltage during the flat-top period. Figure 6 shows the vector-sum of the eight cavities. Stability of 0.006% (rms) and 0.024° were achieved in the amplitude and phase, respectively. A digital filter with 250-kHz bandwidth was applied to reject the 8π/9 mode in this measurement [2].

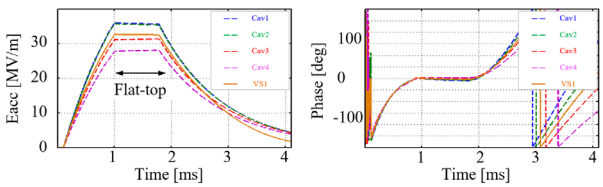

Figure 5: Cavity pick-up signals in the first cryomodule measured by μTCA.4 board (type II).

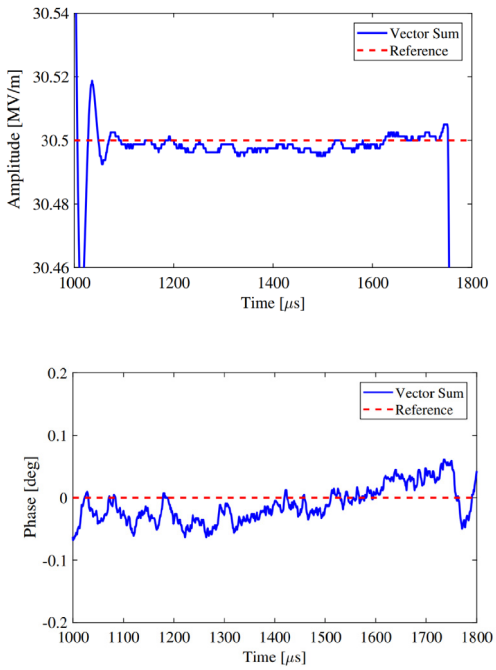

Figure 6: Amplitude and phase of vector-sum for eight cavities during the flat-top period.

An RF monitoring system based on direct sampling technique was installed on the μTCA.0 board (type III), as shown in Fig. 7. The main objective of this system was to evaluate the performance of the fast ADC. The cavity pick-up signal and forward signal was sampled by the fast ADC directly in the absence of down-convertors. By applying the direct sampling algorithm, the amplitude and phase of the RF signals were detected successfully by the type III board. Because the frequency of the ADC input signal was up to 1.3 GHz, the signal-to-noise ratio was higher than in traditional LLRF systems employing down-convertors. The stabilities of the amplitude and phase were approximately 0.1% and 0.1°, respectively. In the STF (and cERL), the system was also used to monitor the long-term drifts of the master oscillator and local oscillator because it is not affected by the characteristics of the down-converters [2].

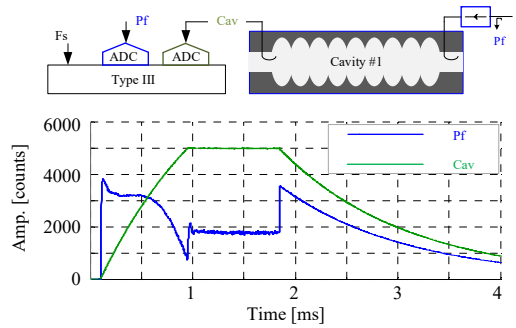

Figure 7: RF monitor system based on the μTCA.0 board (type III).

CONCLUSION

Three types of μTCA boards were developed and applied in the LLRF systems of the cERL and STF. The numbers and types of the digital chips (ADC, DAC, and FPGA) were selected according to the applications of the boards. The EPICS protocol was embedded in the boards for data communication. The performance of the LLRF systems fulfilled the requirements of cERL and STF (ILC).

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