A FRAMEWORK FOR DEVELOPMENT AND TEST OF xTCA MODULES WITH FPGA BASED SYSTEMS FOR PARTICLE DETECTORS*

T. C. Paiva, L. A. Ramalho, A. A. Shinoda, Faculdade de Engenharia de Ilha Solteira, UNESP, Brazil
A. Cascadan†, V. F. Ferreira, M. Vaz, Núcleo de Computação Científica, UNESP, Brazil

Abstract

This work describes a framework to develop firmware for ATCA carrier boards with FPGA. It is composed of an ATCA IPMI protocol implementation for environmental monitoring and control, and a companion XVC protocol implementation for remote FPGA configuration and system debugging. A study case is also presented of the development of a setup to validate a Level 1 Tracker Trigger System proposed for CMS at HL-LHC.

INTRODUCTION

The ATCA standard, originally created for the telecommunication industry, has recently aroused the interest of other fields. In the physics community the ATCA is already been used [1, 2], due to the high level of support to system monitoring and control it provides [3]. As an example, the ITER experiment developed a modular control and data acquisition systems designed on ATCA platform [4]. Also, the LBNL synchrotron built an ATCA readout system with an ATCA processor blade which performs image descrambling and formatting [5]. And, recently, the ATLAS Cathode Strip Chamber (CSC) back-end readout system has been upgraded to ATCA environment with high speed links, commercial Pigeon Point IPMC and Timing Trigger and Control (TTC) I/O for synchronization [6].

ATCA standard is also the choice of the AM+FPGA group to the development of a Level 1 Tracking Trigger (L1TT) system for the Compact Muon Solenoid (CMS) operating in the High Luminosity LHC [7]. Sao Paulo Research and Analysis Center (SPRACE), as part of this international collaboration, is in charge of building a demonstration framework to validate those R&D prototypes. It consists of two ATCA shelves with custom ATCA carrier boards, named Pulsar 2b [8]. One of them implements the Data Sourcing System, which is an emulator for the Outer Tracker detector electronics output, and the other contains the Pattern Recognition System being proposed.

The L1TT electronics, which will be physically inaccessible during the LHC runs, requires safe and reliable operation, remote configuration and JTAG tests of all its FPGA devices. These requirements are attended by our framework, as it follows Intelligent Platform Management Interface (IPMI) [9] and Xilinx Virtual Cable (XVC) [10] specifications, and also it uses Pulsar 2b ATCA carrier boards. The following will describe the implementation of this system and its application in the demonstration setup.

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† cascadan@ncc.unesp.br

ATCA AND IPMI

The ATCA is a standard defined by PICMG [3] that specifies a chassis system (shelf) intended to provide a comprehensive and reliable environment for hosting carrier boards and their extensions, such as mezzanines and transition modules. It defines also the concept of Hardware Platform Management (HPM) consisting of a distributed control system, which relies on the IPMI specification. Controllers collect information from different types of sensors spread in the system and take actions, like speeding up cooling fans or shutting down modules, to ensure a safe environment for the electronic boards. HPM also enables hot swap operations to allow replacement of electronic units with the system powered on. There are three types of controllers in this architecture:

Shelf Manager Controller (ShMC): it is the central element in the shelf, located in the Shelf Manager (ShMC) board, that gathers information from the installed hardware, generates alarms and controls power supply and fan speed.

Intelligent Platform Management Controller (IPMC): it is installed on each carrier board and is a local HPM agent, directly conneted to ShMC.

Modular Management Controller (MMC): it is the simplest management agent residing in the extension modules of the carrier boards, like Advanced Mezzanine Card (AMC) and Rear Transition Modules (RTM), that is only able to execute basic commands sent by the IPMC.

The HPM management elements connect to each other using the Intelligent Platform Management Bus (IPMB) as a physical layer for the IPMI communication [11]. IPMB-0 stands between the ShMC and IPMC cards and IPMB-L connects IPMC and MMC devices. The Figure 1 shows the controllers and the connection betweeen them inside a shelf.

The starting point of the framework was the Pulsar 2b carrier board with an IPMC card already used for simple tasks but with no support for IPMI operations. The previously chosen proprietary real time operating system, RTX from Keil, prevented the use of open source projects as base of the IPMI solution, like CoreIPM, and it was decided for an implementation from the scratch, with a very minimalist approach. It proved necessary support for the hot swap

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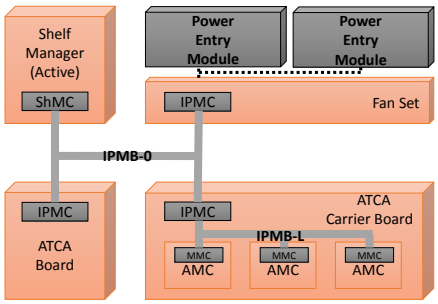

Figure 1: ATCA distributed management consisting of the ShMC, the IPMC and the MMC controllers, and their interconnections through IPMB-0 and IPMB-L buses.

procedure to allow the ShMC to recognize the board when plugged and monitoring capabilities [12].

The ipmb_traced tool was used to sniff the IPMB-0 message exchanging. Carrier boards found in the market served as a reference during the development to harness the understanding about the IPMI specification and to select the minimal set of IPMI commands needed [13].

During extensive tests, the IPMI implementation for the Pulsar 2b IPMC demonstrated its capability to entirely map all the sensors and to efectively handle hotswap operations. Those functionalities allow the ShMC to recognize the carrier board, executing power negociation and fan speed control in response to the sensor reading gathered [13].

REMOTE ACCESS

The programming and debugging of FPGA components is done through its JTAG interface, and standard ports available on computers must be translated to the JTAG protocol. Once an ATCA backplane interconects carrier boards, as shown in Figure 2, ATCA network switches can be used to provide remote access. The XVC protocol [14], specified and supported by Xilinx, defines the translation between TCP/IP frames and JTAG signals, which fits very well for this case.

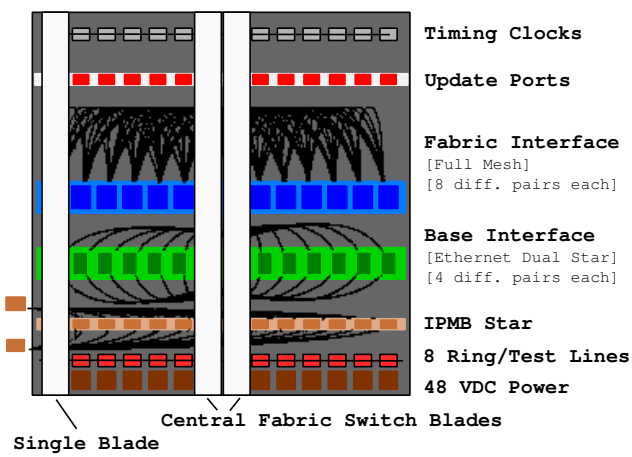

Figure 2: ATCA switch provides external access to FPGA devices on the carrier boards through shelf backplane. [15]

Since the IPMC is connected to the base interface and also is part of the JTAG chain, according to the Pulsar 2b design, the implementation of an XVC service was straightforward. Therefore, the connection between Xilinx device tools and the Pulsar 2b FPGA was made possible by a Vivado Hardware Server instance acting as a gateway for remote programming and debugging.

The ATCA switch also provides fabric interfaces that enable directly communication with the gigabit transceivers of the Pulsar 2b FPGA. This grants flexible write and read channels to the board for data exchanging, as it is the purpose of the IPbus protocol [16], which runs over UDP/IP. Both XVC and IPbus connections implemented for this project are illustrated in Figure 3.

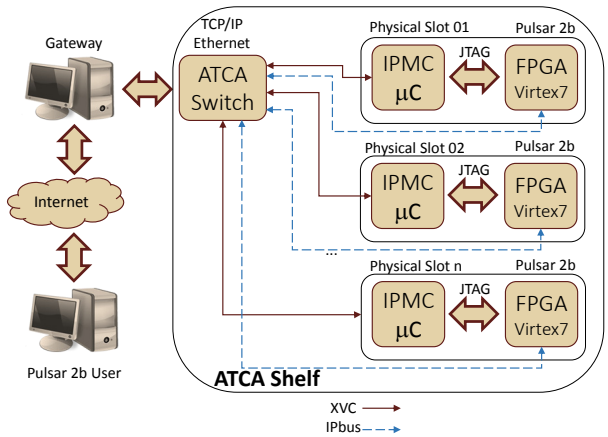

Figure 3: Connections between developer and FPGA using the XVC service and IPbus.

FRAMEWORK APPLICATION

In the L1TT demonstration, the Data Sourcing system deliver data as the real system, with an user interface with IPbus connection to a computer [16], writing and reading data in a dual port memory and executing commands like start and reset.

The computer also controls the Timing, Trigger and Control (TTC) LHC sync system that provides a common clock source and the BC0 (LHC orbit flag 11 KHz) signal to synchronize all boards in different shelves. The data stream from Data Sourcing Shelf to Pattern Recognition Board happens at the same time in all links, as shown in Fig. 4.

The data transfer happens using a wrapper interface, which provides the transceiver user clock, data valid and data input signals. The wrapper is a high speed serial link protocol that can be performed by any differential protocol and encoding system. For the first shelf level tests, it was used the Gt Wizard 64b66b protocol [17] as a wrapper to connect the Data Sourcing Shelf and the Pattern Recognition Board.

We applied a tuning process to improve the performance of the channels to achieve higher speed links without losing reliability. The process was performed using the Xilinx

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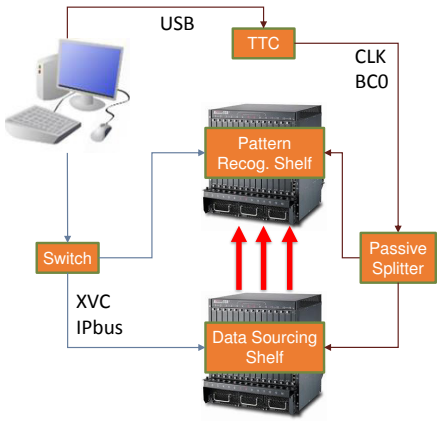

Figure 4: Shelf level test demonstration setup.

IBERT tool, which allows the developer to measure the bit error rate (BER) and eye scans while applying pseudo random binary sequences to stress the channels. Therefore, it is possible to equalize the channels changing their tuning parameters, e.g. TX Differential Swing Voltage, and check their influence in the errors measured.

As result, we found a tuning setup for channels in 8 Gbps that provides a BER in the order of 10^{-12}. The quality could also be checked in the eye scan blue open area in the Fig. 5. The reliability reached meets the requirements of the L1TT demonstration.

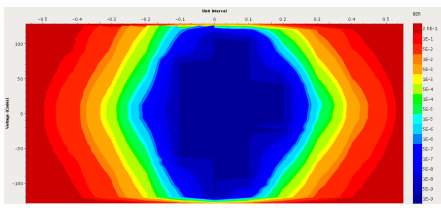

Figure 5: Eye scan of a L1TT demonstration channel.

CONCLUSION

The IPMI service implemented for the Pulsar 2b IPMC enables the carrier board to operate in a safe and optimal condition inside the shelf. When the Data Sourcing System pushes the data rates to the limit, the FPGA devices tend to overheat, which is prevented by the ShMC adjusting the fans speed according to the sensors reading. The ShMC is also able to deactivate the boards in dangerous situations, as in power surge events or temperature excessive rises. With the XVC service, it is possible to remote program and debug FPGA devices in an intercontinental connection. The remote access also allows the collaboration to share the hardware infrastructure available, saving both resources and time.

The Data Sourcing shelf emulates the Tracker detector output, sending off-line simulated pre-trigger data through links synchronized with the help of LHC TTC clock. The platform proved to deliver event data with a error rate low enough for the tests purpose, at 8 Gbps for each channel resulting approximately 32 Gbps per link. Future work will improve the data rate communication and also will define better constraints for the framework operation, which will assist the L1TT Demonstration in several aspects.

REFERENCES

[1] V. Bobillier *et al.*, "MicroTCA and AdvancedTCA equipment evaluation and developments for LHC experiments," in: *Journal of Instrumentation* 11.02 (2016), p. C02022.

[2] R. S. Larsen, "Recent Progress in Next Generation Platform Standards for Physics Instrumentation and Controls," in: *18th IEEE-NPSS Real Time Conference (RT)* 1.1 (June 2012), pp. 1–5., *n 3.0 AdvancedTCA Base Specification"*. 2008.

[4] M. Correia *et al.*, "Development of High-Availability ATCA/PCIe Data Acquisition Instrumentation," in: *IEEE TRANSACTIONS ON NUCLEAR SCIENCE* 63.3 (June 2016), pp. 1620–1624.

[5] P.Mcvittie *et al.*, "A Readout System for High-Speed CCD Cameras Based on Advanced Telecommunications Computing Architecture," in: *IEEE Nuclear Science Symposiwn and Medical Imaging Conference Record (NSS/MIC)* 1.1 (2012), pp. 1623–1625.

[6] R.Claus, "A new ATLAS muon CSC readout system with system on chip technology on ATCA platform," in: *Nuclear Instruments and Methods in Physics Research A* 1.1 (2015), pp. 272–274.

[7] TechnicalProposal for the Phase-II Upgrade of the Compact Muon Solenoid. `https://cds.cern.ch/record/2020886/files/LHCC-P-008.pdf`

[8] ATCA at Fermilab, `http://www-ppd.fnal.gov/ATCA/`

[9] INTEL,HEWLETT-PACKARD, NEC and Dell, *IPMI Specification v 2.0*, Tech. rep. Intel, 2013.

[10] Xilinx Virtual Cable product, `http://www.xilinx.com/products/intellectual-property/xvc.html`

[11] P.Perek and D. Makowski, *Intelligent Platform Management Controller for ATCA Carrier Boards*, Ed. by Lambert Academic Publishing, 1st ed. Saarbrucken: Lambert Academic Publishing, 2011.

[12] T.C. Paiva, "Remote Development Environment with Reconfigurable Components in the Advanced Telecommuniations and Computing Architecture Context," MA thesis. São Paulo: FEIS UNESP, Sept. 2016.

[13] L.A. Ramalho *et al.*, "Development of an Intelligent Platform Management Controller for the Pulsar IIb," in: *2015 IEEE Nuclear Science Symposium and Medical Imaging Conference* 1.1 (2015), pp. 1–4.

[14] XilinxVirtual Cablespecification, `https://raw.githubusercontent.com/Xilinx/XilinxVirtualCable/master/README_XVC_v1_0.txt`

[15] Choosingthe Right ATCA Fabric, `http://www.embedded.com/design/connectivity/4009302/Choosing-the-Right-ATCA-Fabric`

[16] IPbus: a flexible Ethernet-based control system for xTCA hardware.

[17] High Speed Serial, `http://www.xilinx.com/products/technology/high-speed-serial.html`

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