

A FPGA BASED HIGH SPEED DATA ACQUISITION CARD

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Abstract

A FPGA based, high speed, two channel, analog input card with a maximum input sampling rate of 1 Giga samples per second (Gsp/s) per channel has been designed and tested. The card has got an on-board cPCI interface but has been designed in a way that it can also work as a stand-alone system. The card can function as a platform for developing and evaluating different FPGA based hardware designs. Recently, the card has been used to develop a direct sampling Low Level RF (LLRF) controller for controlling the electromagnetic fields of a prototype heavy ion RFQ. It has also been tested for acquisition of data in nuclear physics experiments. Pulses from surface barrier and silicon strip detectors were acquired at an input sampling rate of 1 Gs/s employing ²⁴¹Am and Am-Pu sources. The design developed for this makes use of pre-triggering. This paper discusses the functionality, salient design issues and features of the card. Finally the hardware designs of above mentioned applications related to different areas of LLRF control and nuclear pulse acquisition are explained and the results obtained are presented.

INTRODUCTION

A data acquisition system consists of a ADC driver, a programmable data processing and storage unit, and also a data transfer stage. The advent of FPGA and subsequent progress in related technology has enabled the data processing stage to be easily adapted to different applications.

The FPGA based high speed data acquisition card can function as a platform for designing and evaluating different FPGA based hardware designs. Features and design issues relevant to data acquisition are briefly presented. The card has been used to develop a LLRF controller and also has been used to acquire data in nuclear physics experiments. These applications are briefly described.

FUNCTIONALITY & SALIENT DESIGN ISSUES

The card consists of the following features:

- FPGA: VIRTEX-5 XC5VFX100T
- cPCI interface: 32 bit, 33MHz master interface with DMA transfer capability using *PCI 9054* from PLX Technology.
- Clock: 156.25 MHz clock oscillator for SFP; 40 MHz clock oscillator for PCI; 32 MHz system clock; Clock distribution for ADC and DAC.
- Rocket IO interface: Two SFP connectors are provided for SFP modules

- Memory: 2GB DDR2 – SDRAM; 256Mb flash Memory
- Analog Input: Two channels using 12 bit, 1.0 GSPS ADC: ADC12D1000 from National Semiconductor
- Configuration: JTAG Mode; Using On-board Configuration *PROM*.

Analog input data can be sampled and stored in the DDR2 memory. After the memory is filled, data transfer is done using the PCI interface in the DMA mode. The design thus involves sampling of incoming data in ADC (any one channel at a time) and acquiring the digital samples inside FPGA. The digitized data is then stored for further processing. Thus the path of data traversal is from ADC to FPGA to DDR2 to back to FPGA. Afterwards, the data can be processed at a relatively slow speed and then transferred to the PC via a cPCI interface.

The data acquisition hardware design consists of the following hardware entities:

1. Configuration and calibration of external clock synthesizer (**AD9520 -3**)
2. Configuration of ADC (**ADC12D1000**)
3. Data acquisition of digital samples within the FPGA.
4. Sample rearrangement and concatenation for writing to DDR2
5. Write operation to DDR2 memory via Memory Interface Generator (MIG) core [1].
6. Read operation from DDR2 memory via MIG core
7. Rearrangement of samples to obtain the final stream of digital samples.
8. Transferring data via cPCI interface.

The block diagram of the hardware design is shown in Figure 1.

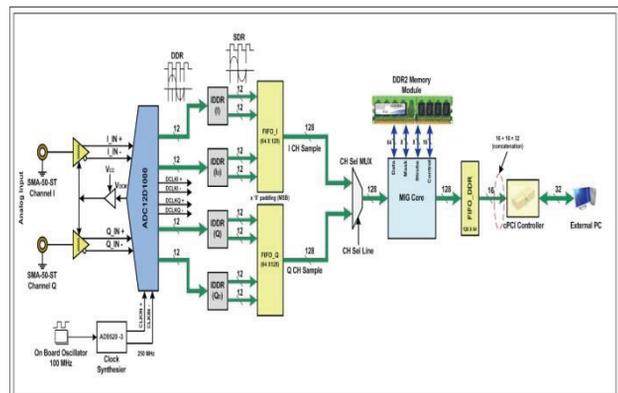


Figure 1: Hardware design for data acquisition.

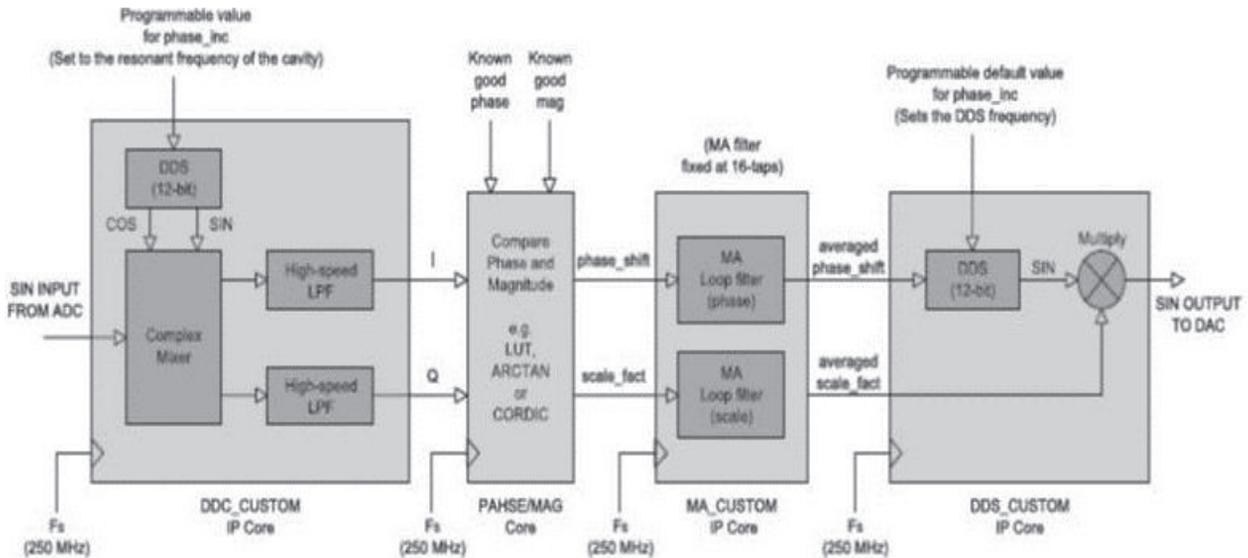


Figure 4: Direct sampling LLRF controller block diagram.

An output reference clock of 250 MHz is provided by the ADC to the FPGA for acquiring data. The data coming from the ADC is **DDR** (double data rate) on all the four buses. Hence the effective data rate is **250 X 2 = 500 MHz** on each of the data bus (refer to Figure 2 and Figure 3 for more details).

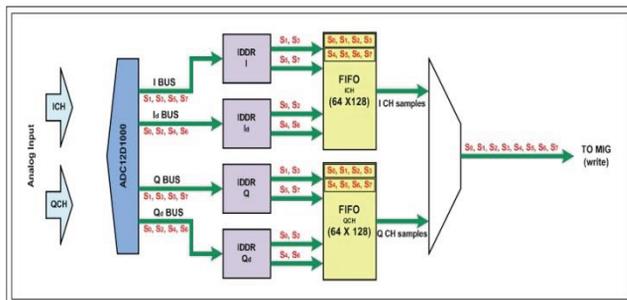


Figure 2: Sample interleaving before write operation.

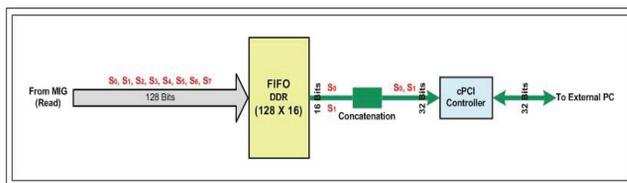


Figure 3: Sample interleaving before read operation.

Data acquisition inside FPGA is done at a speed of 250 MHz clock frequency. ADC provides the reference clock to the FPGA for each channel (I and Q) and one has to latch the samples in on every rising edge of the clock pulse. Initially DDR data is sent by the ADC which is converted to SDR data by using the IDDR primitive. IDDR is used to convert the input DDR data into SDR

data. The output is provided on two separate parallel buses of the ADC for further processing. The hardware design described above is common to all the applications. This design makes available the sampled data for further processing. Data is sampled by the ADC, stored in the DDR2 memory. This memory is then read and the data is processed according to the relevant algorithms typical to the application being developed. The processed data is then transferred to the PC via the cPCI link. In the subsequent section algorithms related to two applications which have been implemented in the FPGA are briefly discussed.

APPLICATIONS

Direct Sampling LLRF Controller

A direct sampling LLRF controller hardware design has been developed for the 75 MHz heavy-ion RFQ (as shown in Figure 4). This design digitizes the pick-up of the resonant cavity, detects the In-phase (I) and In-quadrature(Q) components, generates the phase and amplitude error signals and finally generates a sine wave output signal which when converted to the analog domain using a DAC can be amplified. This signal then can drive the resonant cavity.

The design consists of the following hardware components:

- Direct digital converter(DDC)
- Phase and magnitude compare (PMC)
- Moving average loop filter(MA)
- Direct digital synthesizer(DDS)

The DDC entity performs the digital mix-down of the cavity pick-up input signal to baseband. It also generates the internal I/Q samples. The *phase_inc* value controls the internal DDS frequency and should be set to the resonant

frequency of the cavity. Assuming a resonant frequency of ~ 75 MHz, after the digital mix-down this will generate tones at DC $(75-75) = 0$ Hz and also at $75+75 = 150$ MHz. At a sampling rate of 250 MHz then the unwanted secondary tone at 150 MHz will also have an alias at 100 MHz $(250-150)$. To this end, the high-performance FIR low-pass filters have been designed to block any frequency above 25 MHz.

The PMC entity generates a known good phase and amplitude from the detected I and Q components. This is done with either the CORDIC algorithm, using the arcTan function or by Look-up-Table approach. The output of this entity is the phase and amplitude scale factor information.

The MA entity acts as a loop-filter. The purpose of this entity is to prevent abrupt changes to the *phase_shift* and *scale_fact* signals which may cause instability or oscillation in the loop. A simple moving-average filter has been implemented with 16-taps. The number of taps is currently fixed, but we can modify this if necessary.

The moving-average filter also has the secondary effect of being a low-pass filter.

The DDS entity generates the output sinusoid waveform. The core uses a 12-bit LUT and has a programmable *phase_inc* input that controls the frequency of the output sinusoid. The component also has additional *phase_shift* and *scale_fact* inputs that can control the relative phase

and amplitude of the output signal. The *phase_shift* input is a 32-bit unsigned value. The full 32-bits represent a shift of 360° . The *scale_fact* input is a 16-bit scale factor that scales the output waveform. It is a signed value in s1.14 format.

This hardware design has been implemented in the FPGA. Individual components have been successfully tested.

Pulse Acquisition

Pulses from surface barrier and silicon strip detectors were acquired at an input sampling rate of 1 Gs/s employing ^{241}Am and Am-Pu sources. The amplitude spectrum for the Am-Pu source is shown below.

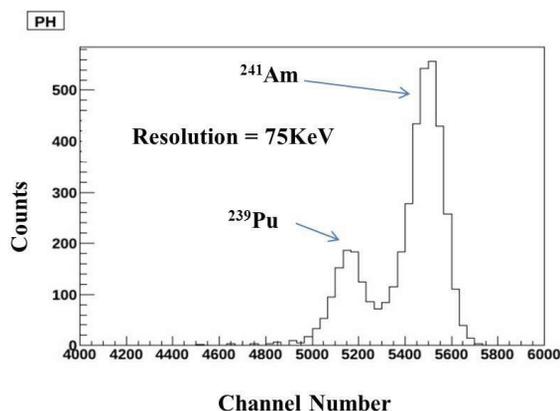


Figure 5: Amplitude spectrum of Am-Pu source.

The design developed for this makes use of pre-triggering. Three trigger modes have been implemented viz. normal trigger, post trigger and pre-trigger modes.

In the normal trigger mode, the data acquisition starts slightly after the occurrence of the rising edge of the trigger.

In the post trigger mode, the data acquisition begins after a programmable number of samples of occurrence of the rising edge of the trigger. The number of samples after which the acquisition should start is determined by the value stored in a register (trigger width).

In the pre trigger mode, the data acquisition starts a programmable number of samples before the rising edge of the trigger comes. The number of samples is determined by another register (pre-trigger width).

The trigger logic has been designed using a circular buffer architecture. A FIFO is used as a temporary buffer to store the samples for pre trigger mode and when the mode is enabled, it starts getting written into. Once the samples are equal to the pre-trigger width value, the FIFO gets into free read/write mode. That is the read and write start at the speed of the data input rate. This makes sure that the fixed number of samples is always in the buffer and they are updated at every clock edge. In post trigger mode, the data acquisition waits for the number of samples written in the respective register for the start for the start of acquisition. Once the samples surpass this value, data acquisition starts. In normal mode, all these are bypassed and the data acquisition occurs at the rising edge of the trigger.

The amplitude spectrum as shown in Figure 5 was generated after acquiring 2GB of pulse data. This data was stored in the on-board DDR2 memory and then transferred via a cPCI link to the PC.

CONCLUSION

The card has been successfully used to implement two applications (viz LLRF controller and nuclear pulse acquisition). For both these applications data was successfully sampled at an effective sampling rate of 1Gps. Individual components of the direct sampling LLRF controller have been successfully tested. Integration and testing of controller is in progress. The Am-Pu amplitude spectrum has a resolution of 75 keV. Development of FPGA based filtering algorithms for nuclear pulse processing is on-going.

REFERENCES

- [1] UG 086 memory Interface generator (MIG), www.xilinx.com