

Using the Advanced Telecom Computing Architecture xTCA as crate standard for XFEL

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DESY – MCS

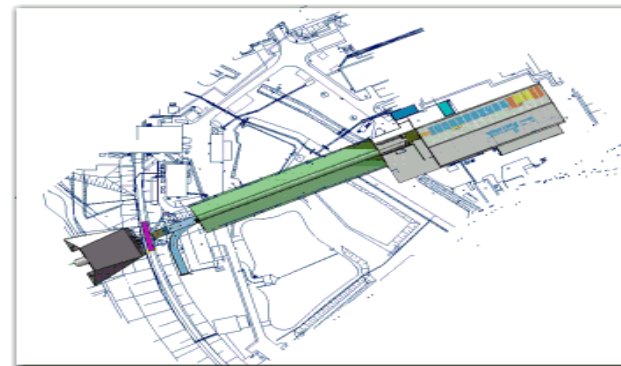
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**Working in the controls group
for FLASH and XFEL**

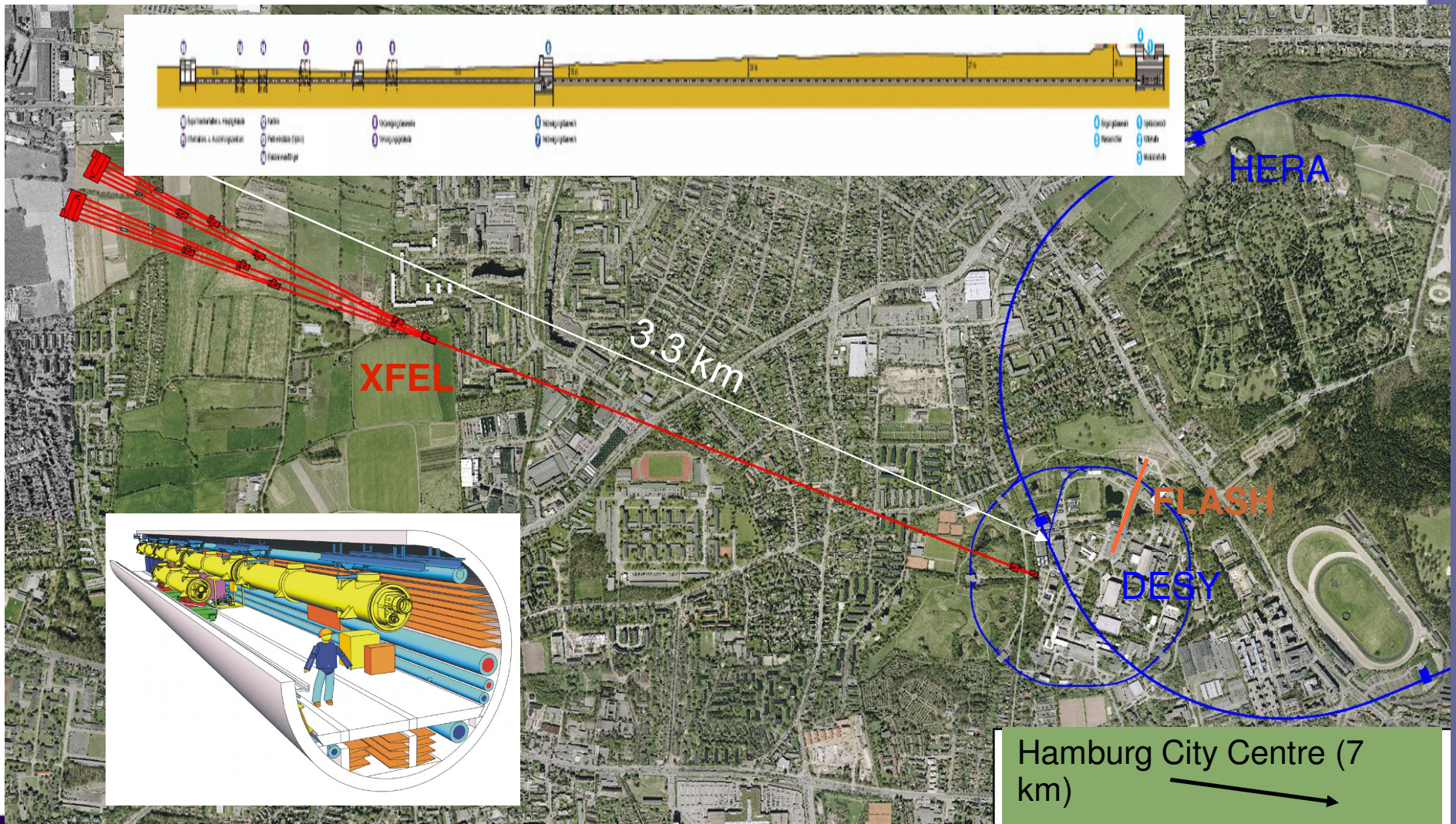
FLASH



- Linac is 280 m long
- up to 1 GeV energy => ~6 nm Photon beam
- 2.5 kA peak current
- 5 Kryo Modules with eight 9-cell cavities
- 4 Klystrons to drive Gun and Modules
- VUV FEL light down to 6 nm wavelength
- Undulator length is almost 30 m
- shared between Users, XFEL and ILC
- Prototype for XFEL and ILC



X-Ray Free Electron Laser (XFEL)



X-ray Free Electron Laser



- an European project at DESY
- Linac will 1500 m long
- up to 25 GeV energy
- ~100 Kryo Modules with eight 9-cell cavities each
- 1 Klystrons to drive 4 Modules
- 1.3 GHz operation
- XFEL photon beam down to 0.1 nm
- German government announced to spend 50% of the budget
== ~350 Mio Euro
- start of civil engineering in 2009

DOOCS features

- Distributed Object Oriented Control System
- Client / Server system with ONC-RPC
- Implemented mainly in C++
- Local HDD for archiving and configuration
- Every server has its local .conf and .log file
- Hierarchical name space
- Name calls -> query all locations or properties
- Most source of a server is inside a central C++ library
- No central DataBase
- For Solaris, Linux and Windows

<http://doocs.desy.de>

DOOCS features con,t

- Tight connection to the DOOCS DAQ
- A common client C++ API for
 - ➔ DOOCS ONC-RPC
 - ➔ TINE
 - ➔ EPICS
- On top of this API
 - ➔ DOOCS Data Display DDD
 - ➔ Generic Applications and command line tools
 - ➔ MatLab
 - ➔ LabView

Poster : TUP010

DOOCS features con,t

- Native Java API : jDOOCS
 - ➔ talking to : DOOCS, TINE, Tango, (Epics planned)
- On top of this API
 - ➔ jDDD
 - ➔ Alarm & Info System
 - ➔ jDTool (generic access)

Motivation

- ~300 Crates are required inside XFEL
- We want a manageable and reliable system
- Find today a solution with support for the next 10 years
 - Cheaper solution as VME
- Common Hardware and Software standards for all subsystems
 - Is xTCA the right platform for XFEL?

Why crates at all ?

- 10 Hz operation at XFEL
- single bunch resolution over the whole macropulse
- very fast analog channels
- about 130 analog I/O channels per RF station
- short cables to the diagnostics devices
- remote management

Evaluation of ATCA and μ TCA

- Trying crates and modules from different manufacturers
 - ➔ Is it a 'standard' ?
 - ➔ Learn to specify a big system
- **Design of hardware (AMC)**
 - ➔ Can one understand and implement the specs?
 - ➔ Is the analog (ADC) performance sufficient?
- **Design of software**
 - ➔ FPGA connection by PCIe
 - ➔ Device drivers for LINUX and Solaris
 - ➔ IPMI code for the MMC
 - ➔ System management

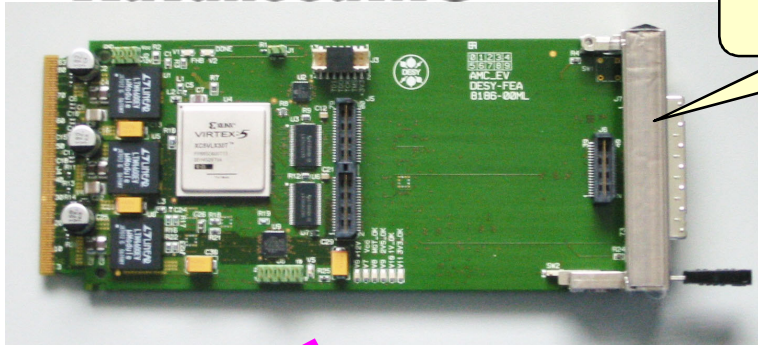
■ ATCA evaluation by the XFEL LLRF group

ATCA features

- ATCA == **A**dvanced **T**elecom **C**omputer **A**rchitecture
 - serial, switched bus (GB Enet, PCI-x)
 - redundant, monitored -48V powersupply
- standardized monitoring and management (IPMI)
 - complete redundant setup possible
 - no IO from industry yet
 - too expensive for now

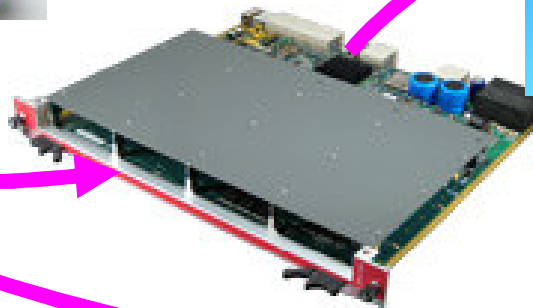
Hardware: xTCA

AdvancedMC™

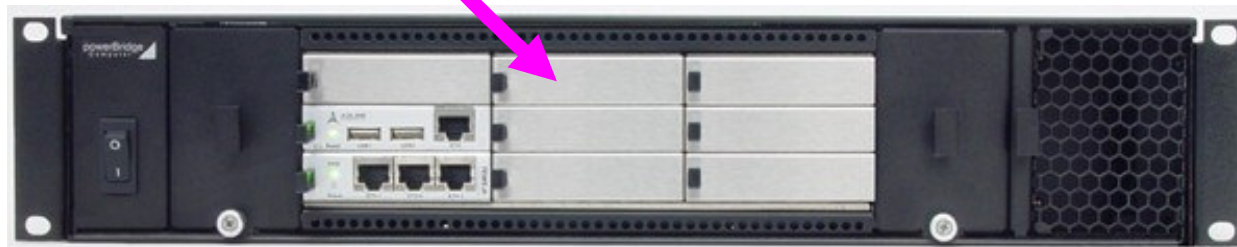


Timing receiver
board size

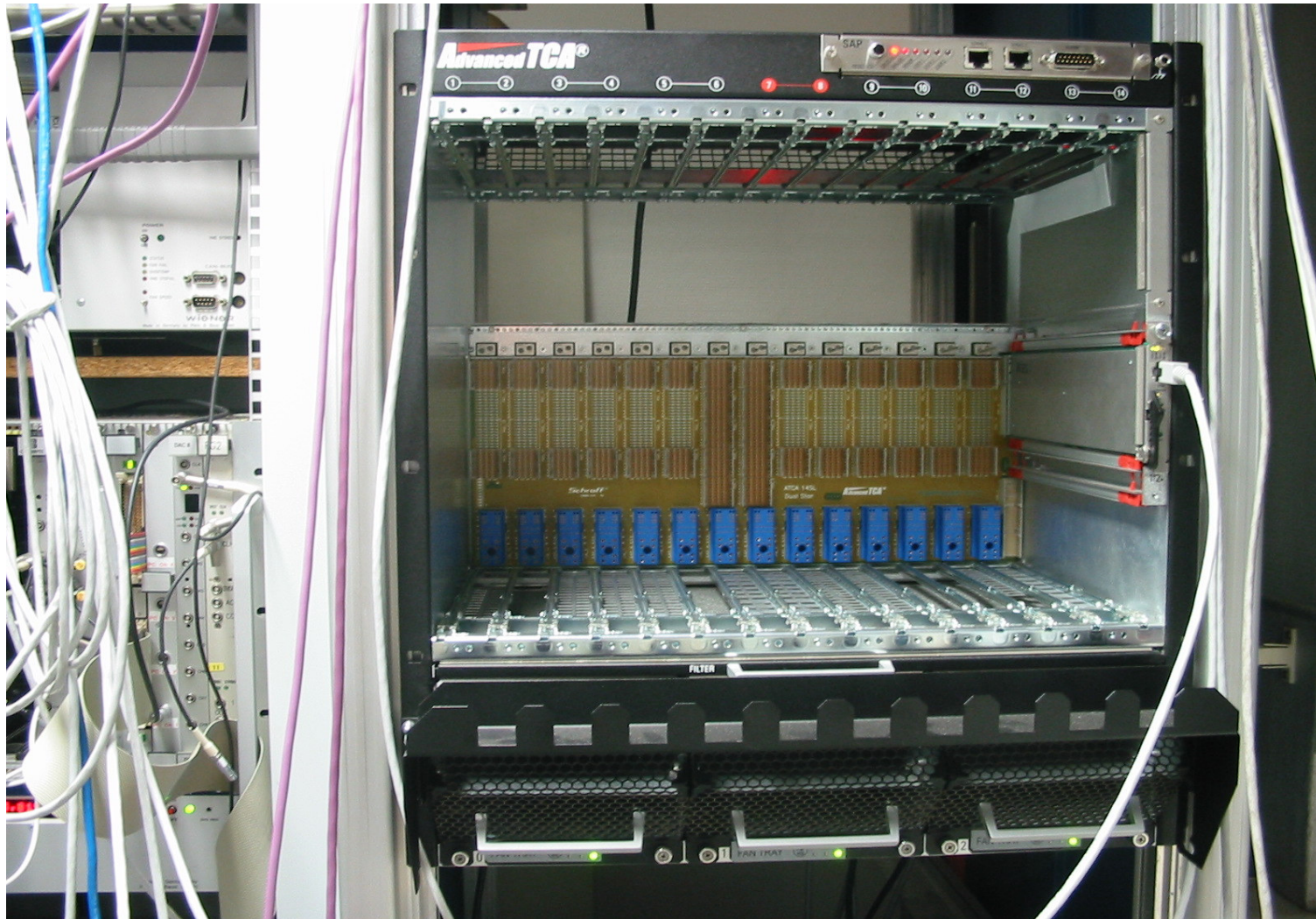
AdvancedTCA®



μTCA™



Future Shelves : ATCA



μ TCA shelf

12 slot



4 slot



8 slot
low cost
active backplane



double size:
12 slot



6 slot

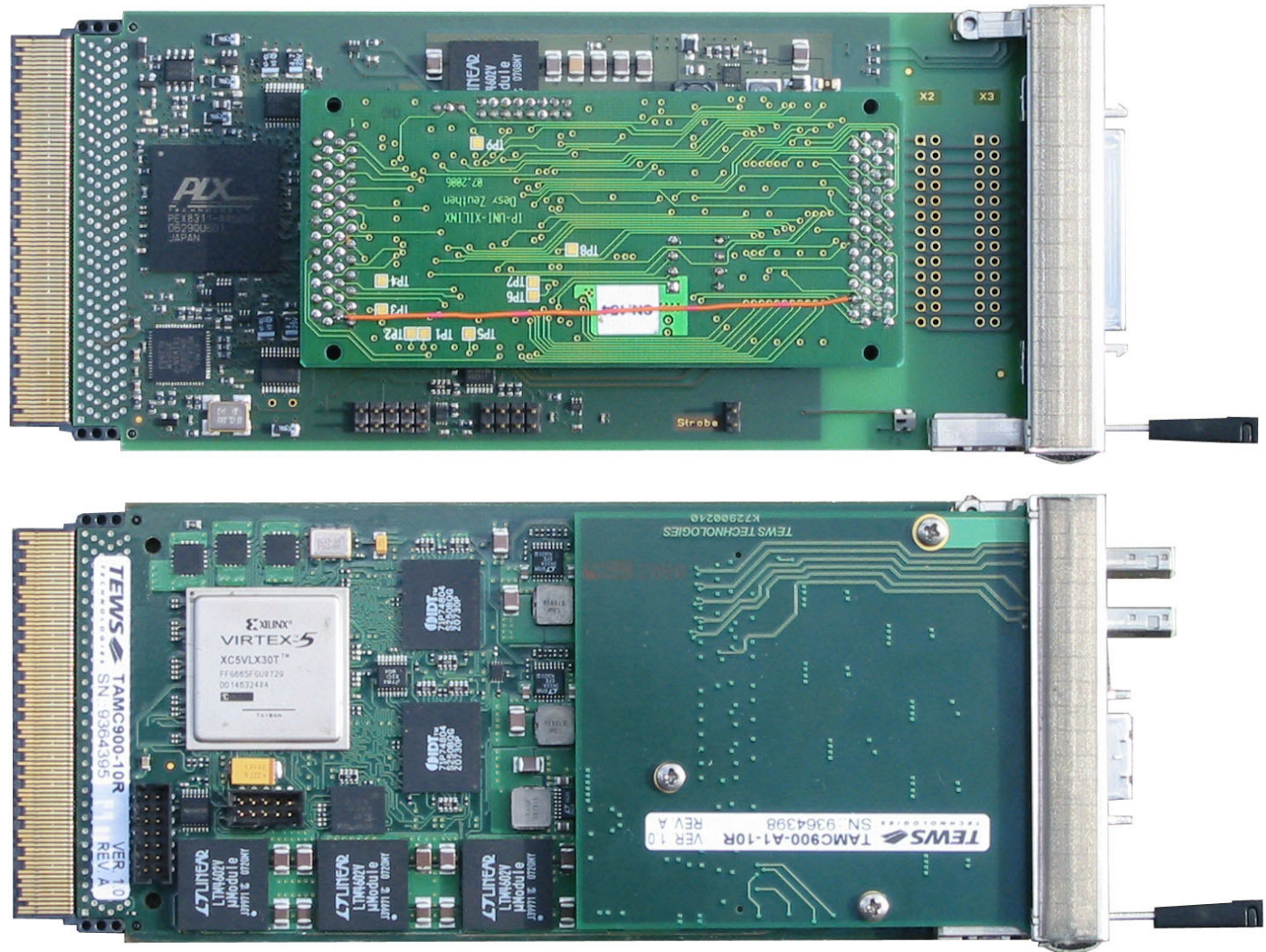


standard AMC's

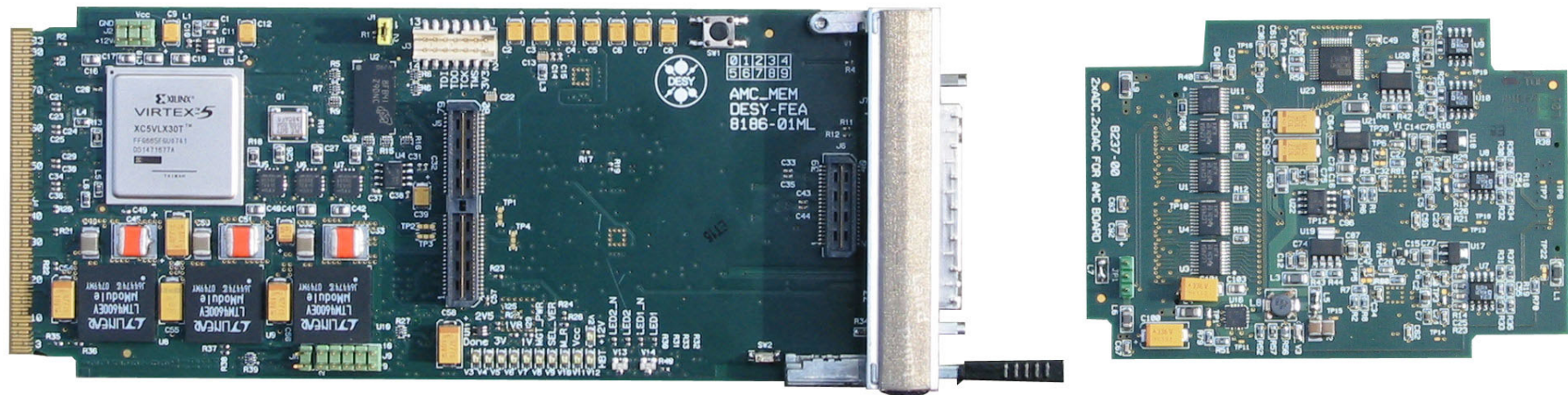
IP carrier to
connect e.g.
legacy
FLASH timing

A solution to
connect IO
to μ TCA

ADC:
8 channel
100 MHz
14 bit,
design contract
with Tews



DESY AMC

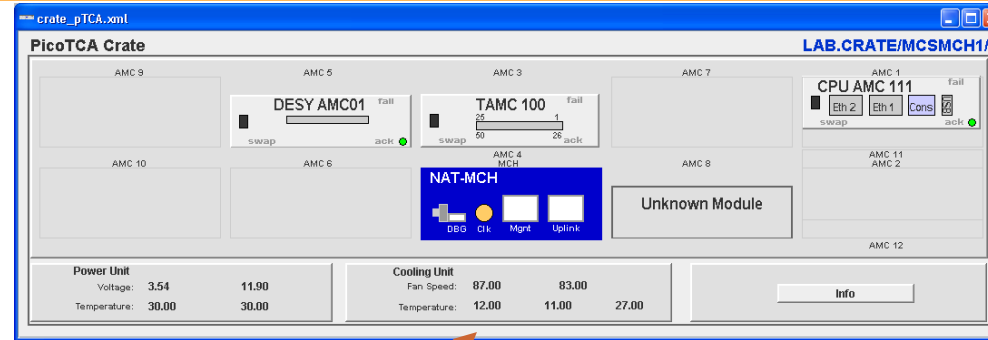
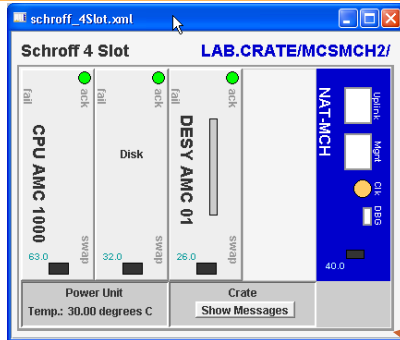


- Development of an 'universal' AMC module
 - ➔ Hardware design with Virtex5 and 256MB DDR2 SRAM (1GB/s)
 - ➔ FPGA code development with PCI Express interface and DMA
 - ➔ 370 MB/s into user space (128byte payload size)
 - ➔ DOOCS server and OS driver
 - ➔ IPMI code for 'Module Management Controller' (Atmega-128)
 - ➔ Piggyback with 2 ADC and 2 DAC channels, 100MHz

IPMI for DESY AMC Board

- IMPI code on Atmel-128
 - ➔ Implements version 1.5 functions
 - ➔ FPGA code loading in preparation
- IPMI control system integration
 - ➔ DOOCS server for ATCA, μ TCA and computers
 - ➔ IPMI communication via Ethernet to the crates
 - ➔ Extracts from IPMI the available information
 - ➔ Creates a dynamic list of AMC modules
 - ➔ Creates a dynamic list of sensors
 - ➔ Archives values and provides reset/boot commands to FPGAs or CPUs
- ➔ Required configuration: one entry per crate (IP name)

DOOCS integration



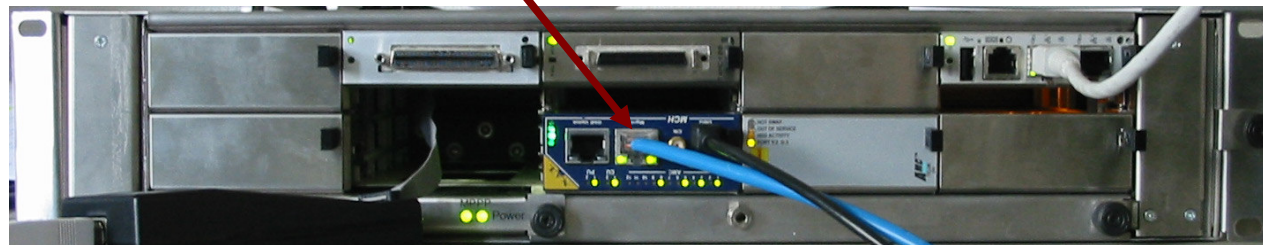
jddd

**JAVA
Application**

DOOCS

DOOCS Server
automatic configuration from IPMI

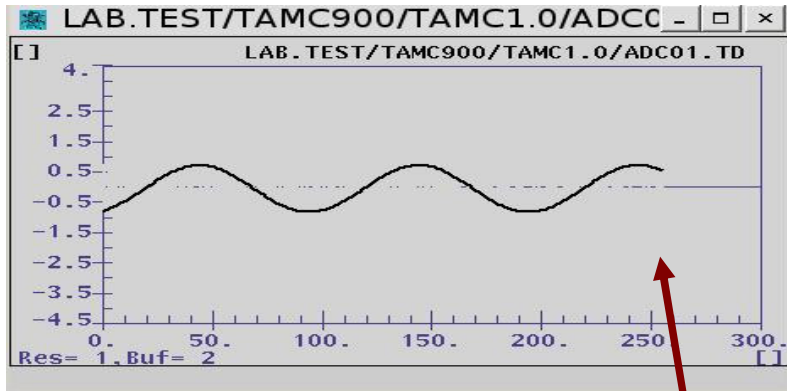
IPMI over Enet



DOOCS integration

2 Mhz Sine wave sampled with 100 MHz

FLASH Timer Server



TTF Timer:		MCP1							
Ch #	On/Off	Event #	Div.	P-Width	Delay/ms	Description		Pre Scale	
N0	EN	A6	9MHz	770NS	+ 3.1110	MCP 1-4 trigger	OFF	9MHz/	1 2 4 9
N1	EN			770NS	+ 3.1097	Flash Lampe trigger			
N2	EN			770NS	+ 3.1109	MCP 5 trigger			
N3	EN	A6	9MHz	770NS	+ 6.5654	ADC_server SIGUSR1	OFF	MSK	FLAG
N4	EN			770NS	+ 55.4540		OFF		
N5	EN	B7	1MHz	770NS	+ 65.0000	ADC_SERVER SIGUSR2		EVENT: 250F215	
N6	EN	A6	9MHz	770NS	+ 3.1158	ICCD trig. SFPD (R.T.		ms: 199	SIGUSR1
N7	EN			770NS	+ 3.1164	Scope trig. SFPD (R.T.	OFF		

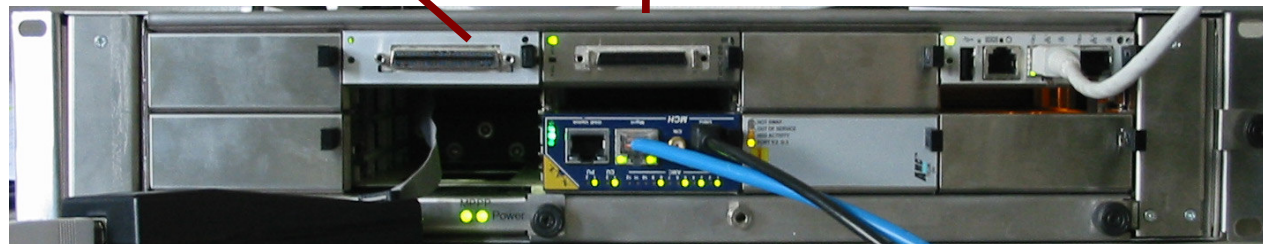
DOOCS

ADC server
Running on AMC CPU

DOOCS

FLASH Timer Server

ADC data via PCI Express



Experience (Problems)

- **Modules are not enabled if IPMI returns wrong stuff**
 - ➔ e.g. protocol version 1.0 string (instead of 1.5 or 2.0)
- **Payload Power MUST be switchable**
 - ➔ Otherwise: MCH init and CPU booting conflict
- **Fan speed control important**
 - ➔ Especial for development crates on a desk
- **Backplane configuration not standard**
 - ➔ MCH, CPU and backplane must fit together
- **CPU should have network (PXE) boot feature**
 - ➔ Important for large installations
- **PCB with traces too close to the edge can be destroyed**
- **Dynamic configuration of PCIe**
 - ➔ OS driver handling; board with one lane was seen by CPU with 4 lanes

Experience (Pros)

- **Management of crates is well defined**
 - Dynamic module and crate info
 - Gives all relevant info
- **Fast data transfers (>400MB/s on 4 lanes PCIe)**
- **Hot-swap**
 - hardware is controlled by the MCH - **great!**
 - software reconfiguration of OS PCIe drivers to be done
- **Good decoupling of modules on the backplane**
- **Good analog performance**

Thank you