EMBEDDED DEVICE CONTROLLERS

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Abstract

The embedded device controller network is seen as an open-source, two tier framework that allows device controllers to control distributed devices at a 5 KHz rate. This network provides timing and data transmission to support a network of up to 300 input devices to be read into 30 cell controllers, resolve a 300x300 control matrix in portions, sent the new outputs to the controllers and settle in 200 micro seconds. It also support identification of systems conditions in under 20 milliseconds. This paper discusses the plan for development, characterization, and deployment.

INTRODUCTION

To provide this comprehensive monitoring, control, and automation, the NSLS-II control system must scale to support 100,000 physical I/O connections and 350,000 computed variables that can be correlated to analyze events and provide data for all control aspects. It must support 1 Hz model-based control, 110 kHz power supply digitization, 500 MHz RF control, 5 KHz orbit feedback, and 20 millisecond equipment protection mitigation. It also must provide 5 Hz updates to operators of up to 1,000 chosen parameters, provide coherent turn-by-turn orbit data for up to 2^{10} = 1,024 consecutive turns (for FFT), archive up to 6,000 parameters at a rate of 0.5 Hz continually, latch the last 10 seconds of data from all parameters in the storage ring when a fault is detected in the Machine Protection System (MPS), archive up to 1,024 consecutive turn by turn data for 1,000 parameters at a rate of 10 Hz, and provide pulse-to-pulse beam steering in the linac at 1 Hz.

REQUIREMENTS

Machine control supports linac control that is synchronized to the master timing system to fill the booster ring with 80 nanosecond pulse trains made up of 40 micro bunches of 2 ns length each. Pulse-to-pulse timing jitter will be less than 80 ps at the 1 Hz rate. The pulse is ramped up to the correct energy in the booster ring over 400 ms. It is then injected into the storage ring. The revolution rate for the booster and storage ring is 2.6 μs. Manual control of orbit trims, quadrupoles, sextupoles, and insertion devices is asynchronous. These are controlled by the operators, accelerator physicists, high level applications, or users. In particular, ~10 Hz write/read is suitable for "turning knobs" for a power supply. The only "fast" process is the fast orbit feedback system with 5 KHz bandwidth (and feedback systems for coherent bunch instabilities of order MHz). To summarize, the beam bunches in the ring and the injection process are synchronous to the RF, but everything else has its own time scales. Model-based control is used to correct steering, the orbit, tune, linear chromaticity, optics, etc. in the storage ring at 1 Hz.

EQUIPMENT INTERFACES

The equipment interface will provide the physical connection to the equipment being controlled through a variety of interfaces. The preferred standards will include VME because of physical and electrical performance, Compact PCI or PCI Express where higher performance backplanes or lower point count make this more cost effective, and PLC I/O for applications where equipment safety is required and speed is not. The control system includes all VME crates and processors, any network hardware required for integrating instrumentation, the timing/event system, all hardware used for fast feedback, and all the crates and processors used to integrate the I/O. Except where noted, the intelligent device controllers, I/O, and PLCs are provided by the subsystem. The notable exceptions are the controllers for the undulator equipment and the non-BPM diagnostics in the Storage Ring. The network cables and cables to implement the global buses are the responsibility of the control system.

CONTROL SYSTEM ARCHITECTURE

The primary architecture of EPICS supports an Ethernet based communication between clients and servers. This is able to support all conventional client communication for operator support and facility archiving. The control system must provide some global communication that requires lower latency and higher data bandwidths than are available over the Channel Access protocol over Ethernet network. NSLS-II requires: an Event System for synchronizing data acquisition and control; a high-speed data network for providing beam-steering data to all ring power supplies for orbit correction; and a Machine Protection System that is a fast-response bus provided for mitigation against failures

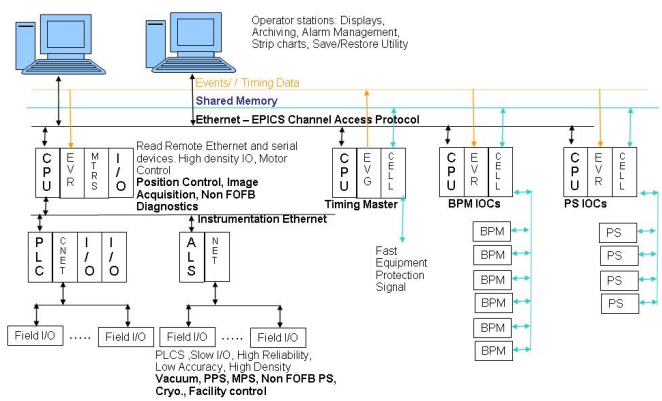

Figure 1: Control System Architecture.

that greatly impact the operation of the facility by either producing excessive radiation or causing equipment damage. We will evaluate the systems available from other laboratories. We are also considering the development of an open-source set of functionality that provides the timing, event, and data communication needed for high speed, distributed applications such as Fast Orbit Feedback and Machine Protection

FAST CORRECTION

Fast correction is not possible through EPICS CA mechanisms because of insufficient bandwidth. It will be realized at the IOC level on separate feedback processor boards dedicated to this function. This involves partitioning the correction calculation across the 30 Steering IOCs to calculate the correction values for the steering elements local to that IOC. Each steering IOC requires access to all the BPM values, to give flexibility in the correction algorithm. This requires a high speed connection to share data between the all 240 BPM devices and 240 Steering Magnets. Two potential solutions for this are to use either reflective memory or fast synchronous communication over dedicated serial lines. EPICS process variables will be used to control the feedback process, by downloading algorithms to the feedback processors and setting coefficients and update rates.

PROPOSED OPEN-SOURCE SOLUTION

Several commercially available components are available to provide this functionality. They are very performant and proven at a number of projects. We are fortunate to be in the position to attempt to develop an open-source platform on which multiple laboratories and manufacturers could develop hardware for low latency (<100 microseconds), high rate (10 KHz), applications. We propose a two-tier architecture that provides low cost (~$150) embedded device controllers that can be

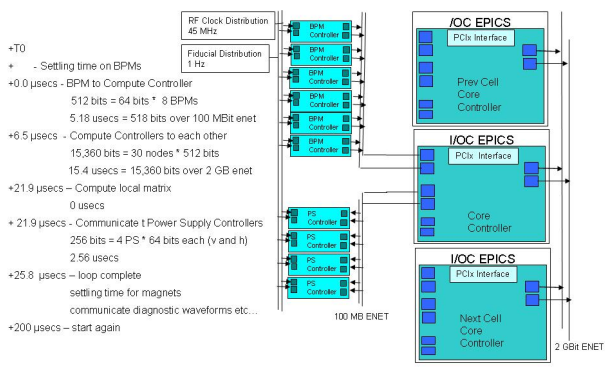

Figure 2: Hierarchical Embedded Device Control.

embedded into the device controllers for little expense. The top level cell controllers manage communication between cell controllers. Each cell controller resolves its portion of the matrix and communicates the new set points to the controllers. These embedded device controllers interface to EPICS through the top level controller that communicates with an EPICS I/O Controller (or any other control system) through a PCI Express interface. The cell controllers are likely to cost in the area of $2,000.00.

CURRENT STATUS

The prototype boards are being developed by Larry Doolittle at Lawrence Berkeley Laboratory working for NSLS 2. A prototype board implements redundant 1.1 GByte Fibers transmitting data with a check character every 8 kbps. There is a master clock synchronizing the communication over the grey wires in the test rig. There is a measured delay between each cell controller of 163 nsecs of latency to transmit through the board. This is a bit behind schedule due to a late start getting funding to the LBL and some delay to appropriate prototype boards. As a result 60% of the funding for 2008 went unspent.

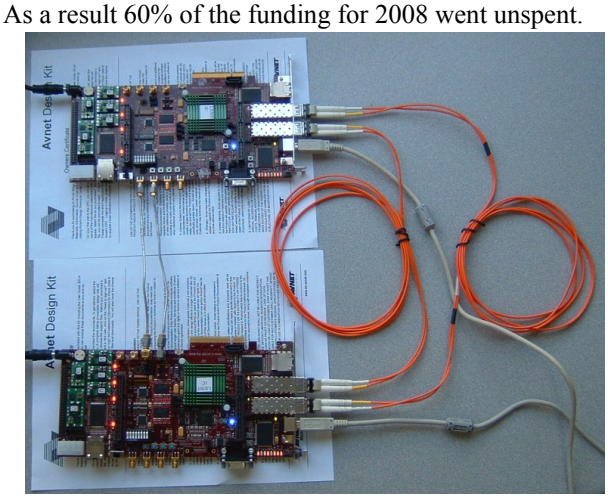

Figure 3: Current State of Prototype.

NEXT STEPS

In FY 2009, which started October 1, we plan to complete the cell controller. The PCI Express interface to the cell controller to communicate from this two tier hardware communication bus into a local processor may be done in parallel. This development supports the integration into EPICS or some other control system environment. The communication for the device controllers will also be completed in FY 2009. Later in 2009, we hope to have vendors and in-house developers integrating the device interface to their BPMs, Power Supply Controllers, Timing, Machine Protection, Top Off Control, and Transverse Feedback. We have kept vendors and other laboratories informed and we expect to have a meeting to discuss the development environment in the first half of 2009.

CONCLUSION

The Open-source, synchronous, device control network is off to a late start. The first results came quickly and look promising. We hope to have the cell controller ready in early 2009. The integration into EPICS can occur in parallel to the development of other hardware. Embedded device controllers should be ready in FY09 for hardware developers to integrate it into their device controllers.

ACKNOWLEDGEMENT

This paper represents the work of Larry Doolittle and Alex Ratti in conjunction with the NSLS II control group to develop an open-source platform for developing and integrating embedded device controllers.