PEP-II BUNCH-BY-BUNCH CURRENT MONITOR*

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Abstract

PEP-II is an asymmetric B-Factory that will have 2200 meter rings storing 9 GeV electrons and 3.1 GeV positrons, each with as many as 3492 beam bunches. To minimize beam-beam instabilities it is important to have equal bunch charge in each ring. This is accomplished by measuring the relative bunch charge and controlling injection timing and intensity. Because there may be a variety of bunch patterns, the bunch monitors are designed to measure beam in every possible bucket. Results of bunch amplitude measurements with a resolution of >9 bits are available to the injection control system at rates up to 66 Hz.

The bunch monitor hardware consists of beam pickups, front end filter/combiners, 1428 MHz down-converters, 1 GHz video detectors, and two VXI systems. In this paper we report on the bunch monitor design .

1 FRONT END ELECTRONICS

Fig. 1 is a block diagram of the Bunch Monitor system.

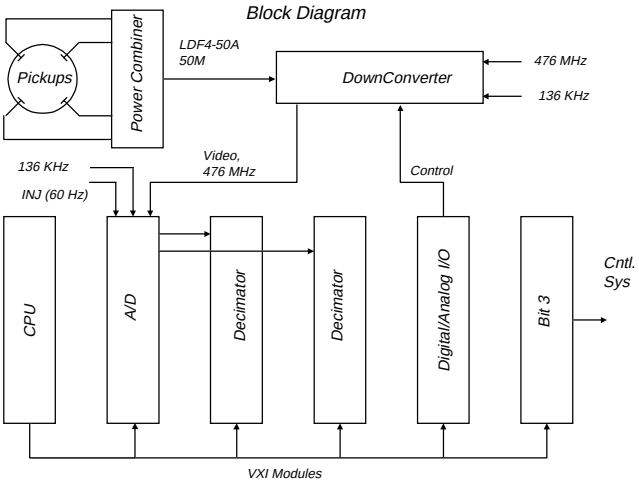

Figure 1 Bunch Monitor block diagram

In both rings the beam bunches are sensed by standard PEP-II BPM buttons, 15 mm in diameter. Bunch signals from these buttons are connected to a nearby filter/combiner chassis. This device consists of four microstrip directional couplers on a common substrate designed for 1428 MHz center frequency (three times the ring cavity RF). The four couplers filter and combine the button signals. Coaxial cables in the chassis are trimmed to eliminate time delay between signals. The pulse doublets occurring 700 ps apart are sent to the Down Converter via 50 meters of ½ inch Heliax™ cable.

1.1 Down Converter

The function of the Down Converter is to heterodyne the 1428 MHz beam signals down to base band video in a bandwidth of DC to approximately 1 GHz. Video output pulses representing the amplitude of individual beam bunches from this module are sent to the VXI electronics A/D converter module. Bunches will normally be 4.2 ns apart, but bucket spacing is 2.1 ns. The video bandwidth must be wide enough to detect the closest bunches.

To maintain phase coherence with the beam signals, it is necessary to synchronously detect the beam signals with 1428 MHz derived from the cavity reference RF. This is accomplished with a 3X frequency multiplier and a high-level doubly balanced mixer. The RF input to the multiplier is phase-adjustable to compensate signal path delay and changes in beam synchronous phase. A 1428 MHz monocycle generator triggered at the ring revolution frequency (136 kHz) is used to simulate a single bunch and is switched into the signal path during setup and testing. The mixer multiplies 1428 MHz against the beam signals. The DC to 1 GHz IF output of the mixer is lowpass filtered to remove high order mixing products. The filter has good pulse response with little ringing.

Charge in a single bunch may vary over 60 dB. A programmable attenuator in the Down Converter is used to adjust bunch signal levels for optimum detection. The A/D converter module input is about ±250 mV full scale. A video amplifier (DC to 1.1 GHz) is used to raise signal levels to the proper level for the digitizer and to provide a video monitor signal for an oscilloscope.

The 1428 MHz center frequency was chosen because of beam pipe size (90 mm). The RF sixth harmonic (2856 MHz) would be preferable because of the required wide video bandwidth, but the pipe diameter permits waveguide propagation of 2856 MHz beam signals unrelated to bunch charge.

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2 VXI ELECTRONICS

An HP E1401B VXI mainframe powers the Bunch Monitor modules. These include a 500 MHz A/D Module, two Decimator Modules, and a commercial low-speed digital/analog I/O Module for range setting and status monitoring. All of the VXI modules are register-based, and are controlled by a 100 MHz Pentium embedded controller running the WinNT 3.51 operating system.

The 1 ns video pulses from the RF Down Converter along with PEP-II timing signals feed into the A/D module. It generates two streams of 8 bit data words at 238 MHz for the Decimators. The Decimators use Field Programmable Gate Arrays (FPGAs) to hardware-sum each bunch 255 times to improve resolution.

The CPU receives a VXI interrupt from the Decimators when the 255 hardware sum is complete. It then copies 3492 x 16-bit data words from the Decimators into local RAM, performs additional sums in software, and then sends the ~8 kbyte results to the PEP-II Control System via a Bit3 VME-VME interface card.

2.1 A/D Module

This module uses the Maxim 101, an 8-bit 500 MHz A/D with a built-in 1.2 GHz sample/hold; this chip is also used on the damping systems at the ALS, PEP-II and the KEK B-factory. The absolute accuracy of this chip is only 6-bits at full speed, but our goal is increased resolution, which is accomplished by summing multiple samples for each bunch. At a 60 Hz injection rate, there is enough time to sum every 2.1 ns bunch 255 times (resulting in a 16-bit sum) and still "decimate" by a factor of 8. Figure 2 is a subsection of a plot showing that, with 256 averages, the effective resolution increases from 2 mV/count to <1 mV/count. With 0 volts input to the A/D Module, the maximum noise peak is also at the 9 bit level .

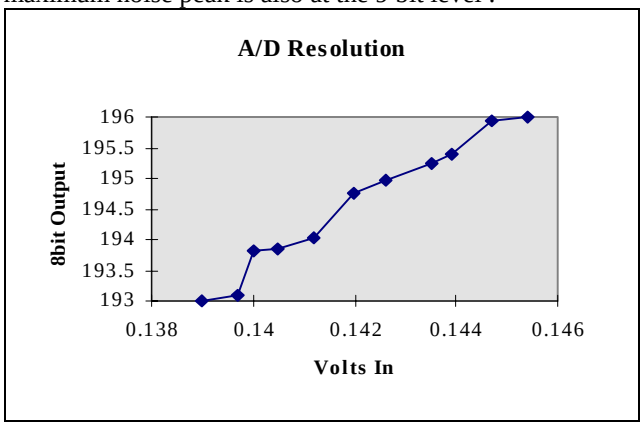

Figure 2 A/D resolution near full scale

The MAX101 continuously outputs two 8-bit output data busses on alternate 476 MHz clock cycles. The VXI A/D module contains a MAX101 evaluation printed circuit board (PCB) (fitted with connectors for clock, data and signal) mounted on a VXI PCB which uses 1 GHz ECL logic (ECLinPS™) circuitry to synchronize the two 238 MHz data streams with SLAC Timing System signals for clock, bunch #0, and injection. The outputs from the A/D module are two 8-bit data streams, the 238 MHz data clock, and a synchronizing pulse. Each stream is sent to a Decimator Module using ELCinPS differential driver/receivers via a custom parallel QuietZone™ cable from Gore Technology.

2.2 Decimator Module

Commercial VME digital signal processor (DSP) alternatives were considered for the Decimator Modules, but no single board could keep up with a 238 MHz data rate; providing synched and decimated data would have required additional design work anyway. Furthermore, we wanted the Decimator to double-buffer each 60 Hz data frame in onboard RAM so that the VXI CPU would have an entire 16 ms to extract the 3492 x 16-bit data across the VXI bus.

Each Decimator uses ECLinPS to split its 238 MHz data stream into 6 separate phased data streams running at ~50 MHz, each stream being responsible for a 291 bunch section of the 1746 total. The number of data streams was chosen based on available Xilinx FPGAs, their speed capabilities, and how many of the appropriate speed-package could be reasonably laid out on a single side of a VXI PCB. Also, 1746 is an even multiple of 6, which makes decimation easier.

The FPGA design would have been much simpler without decimation, but that would have required that read/modify/write (RMW) operations into dual-port RAM be performed in a single cycle. The new XC4000E™ FPGAs have on-chip synchronous dual-port RAM, which would have been perfect for a RMW. Unfortunately, we found no package/speed combination with sufficient RAM to hold the 291x16 bit values required, so we used Integrated Device Technology asynchronous dual-port RAM, which require multiple FPGA clock cycles to do the RMW. We chose 8 FPGA cycles to perform the RMW because it supplied clean control edges for the dual-port RAMs, and [8 x 256 orbits x 7 us/orbit] fits into the 16 ms period. We've also created single-shot FPGA designs that simply write consecutive 8 bit A/D values into the dual-port RAM as a diagnostic test.

A synchronization pulse from the A/D module starts the 6 FPGAs on the accumulation cycle. Each first zeros out 291 dual-port RAM locations, and then performs 291 x 255 RMW operations to this RAM. Upon completion, they toggle the level of an upper bit of the RAM address line; this performs the bank-selection process so that the data from the previous accumulation may be read out from the VXI bus while another accumulation cycle begins.

We investigated commercial VXI interface chips, but they seemed to have more capability (and complexity) than we required, and they are geared towards interfacing Motorola 68xxx processors rather than a slave board. In the end, we built our own VXI interface using a 168-pin

XC4013. It supports the usual register protocol, and also provides two features: first an interrupt service when the accumulator FPGAs signal the completion of an accumulation cycle, and secondly, a register-based address to map the dual-port RAMS into VXI memory space.

Both Decimator and A/D Module VXI PCBs use enclosures from ICS Electronics (Milpitas, CA), which have an elastomeric conductive gasket for EMI shielding.

2.3 CPU and Software

The VXI Pentium embedded CPU was about 6 months away from availability from National Instruments (Austin, TX) when we began software development. In the interim, we used an AT-MXI interface from National Instruments that allowed a desktop PC running WinNT™ to function as the controller. It was extremely gratifying that when the VXI controller did arrive (with WinNT preinstalled, no less), we had it booted and connected to our file server in an afternoon, and the next day it was running the exact same diagnostic LabVIEW™ software to control the Decimators. We did find a difference between the AT-MXI interface and the VXI CPU; the AT-MXI can perform only D16 transfers because of the AT bus width. For full compatibility, it would be better to get the PCI-MXI.

To simplify the VXI interface FPGA, the Decimator design allows access to the dual-port RAM from only A16/D16 space (instead of the more efficient A24/D32 space). Although we realized at the time that this would double the amount of time the VXI CPU would require to move data from the decimator to its local RAM, the CPU specifications suggested this would be small part of the overall time budget. Upon test, we discovered that not only would we have to make twice as many data accesses, but that A16/D16 operations are especially slow for this CPU. In order to keep up with 60 Hz operation, we recoded from LabVIEW™ VIs to MSVC++™ and achieved about twice the speed. The current 100MHz CPU takes about 12.5 ms to perform the data frame tasks, with about 8 ms of this time taken in moving the data across the VXI bus.

3 STATUS

A Down Converter and an HP E1401B VXI mainframe holding the A/D Module, two Decimator Modules, and a commercial low-speed digital/analog I/O Module for range setting and status monitoring has been tested in the lab and installed for the PEP-II High Energy Ring; an identical system will be fabricated for the Low Energy Ring. This system provides a measure of all 3492 bunch amplitudes at rates up to 66 Hz with >±9 bit resolution and noise levels.