FOUR QUADRANT DC TO DC SWITCHING SUPPLY FOR THE FERMILAB MAIN INJECTOR

L. Bartelson, G. Krafczyk, H. Pfeffer, D. Wolff
Fermi Nationl Accelerator Laboratory
P.O. Box 500
Batavia IL, 60510

Abstract

The Fermilab Main Injector (FMI) will require 248 ramped corrector power supplies for the operation of the accelerator. The design and prototype test results will be described in this paper. The 3 main design goals for these supplies are: 1) eliminate failure due to thermal fatigue that has plagued similar systems at FNAL, 2) utilize PWM technology to attain good efficiency and small size, and 3) minimize conducted and radiated noise typically generated by PWM systems. The power supplies operate at 30kHz switching frequency and are rated for +/-150 Volts and +/-15 Amps at 95 percent switching duty cycle and 95 percent efficiency into a 1 Henry magnet load. The FMI requirements call for a ramp cycle of 1 - 2 seconds. During the cycle, the maximum temperature swing, junction to heat sink, of the power components is less than 30 degrees centigrade. The output voltage ripple is less than 1 Volt RMS.

INTRODUCTION

The Fermilab design uses the PWM technology using 4 FETs in an H-bridge configuration for 4 quadrant operation. The switching frequency of 30 kHz was chosen due to accelerator beam interaction considerations. The switching scheme does not use a 50/50 technique. The scheme chosen permits the bottom FET on one side of the H-bridge to be ON continuously. This accounts for less power dissipation since testing showed that the switching losses in the FET are about twice the DC losses. The analog closed loop controls include an inner voltage loop and an outer current loop using a transducer for current feedback. The voltage loop has a response of 5kHz and the current loop has a response of 300 Hz. A block diagram of the unit is shown in Figure 1.

SWITCHING SCHEME

	QUADRANT	
	1 & 2	3 & 4
S1	PWM	OFF
S2	PWM	ON
S3	OFF	PWM
S4	ON	PWM

Figure 2, Switching Scheme

The switching scheme chosen is shown in Figure 2. The FETs on one side of the bridge are pulse width modulated while the devices on the opposite side are held

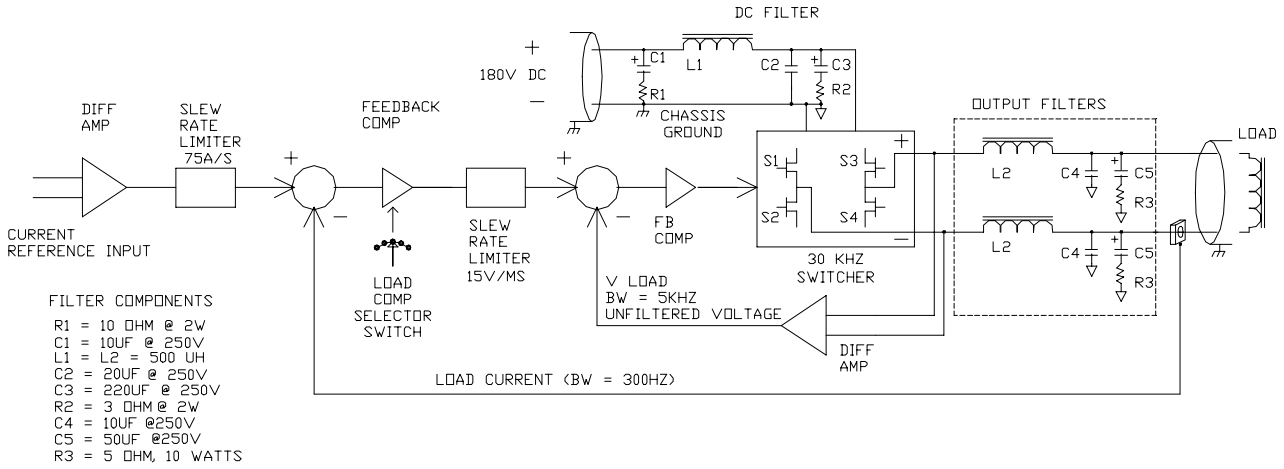

Figure 1, Regulator Configuration

ON, for the lower device, or OFF for the upper . As mentioned above, this technique is used to reduce the switching losses in the bridge. The power dissipation data shown in Figure 3 is for a negative output current of 15 amps, a switching ON time for S3 of 90%, and S2 is ON continuously:

FET	Power (W)
S1	0
S2	20.9
S3	42.6
S4	0.9
Total Power	64.4

Figure 3, Device Dissipation

The data in Figure 3 shows that the switching side has about twice the power dissipated compared to the static side. This is due to the predominance of dynamic switching losses over ohmic losses. Data was also taken with 10 and 50% ON times of the top switching FET operating at 15 amps. In both cases the total power dissipated in the FETs never drops below 50 watts. Power consumed by one filter is 5 watts at 15 amps. The maximum total power in the FETs and the chokes is 74.4 watts. This calculates to be 3.3% of the total 2250 watts of output power.

The FET dissipation was measured in the switching mode using calorimetry. First the case to heat sink thermal impedance was determined for the FETs by operating them in DC mode where power dissipation could be easily measured. Then the case to sink temperature differences were measured while operating in switch mode. The thermal impedance determined under DC conditions was then used to calculate the device dissipation under switching conditions.

Considerable time was invested in getting the temperature data. Copper blocks were added and insulated which made an electrostatic shield between the FET case and the heat sink. This was done because the temperature probes would pick up switching noise that affected the accuracy of their readings. The copper blocks provided more area to clamp thermocouples to and provided a stable time constant for temperature measurements.

FET MOUNTING

Testing was done on different mounting techniques of the FETs and the effects on temperature. The FET used has a TO-247 case with a single hole mount and the case is common to the drain. This obviously requires an insulator which raises the overall thermal impedance. Measurements indicated that a lower thermal impedance on the FET can be achieved if a clamp is used on the case versus the single hole for mounting.

Isolation pads that are commercially available have a large thermal impedance. The combination of a beryllium insulator under each FET and a bar clamp across all 4 devices was the final configuration arrived at. The mounting technique reduced the case to heat sink thermal impedance from 0.85 to 0.2 °C/W. The thermal impedance rating of the FET from junction to case is 0.34 °C/W. Therefore the total impedance junction to heat-sink is 0.54 °C/W. The maximim junction temperature using figure #3 is 42.6 watts times 0.54 °C/W or 23 °C plus the heat sink temperature. A small amount of air flow over the heat sink is needed to limit the maximum junction temperature to 80 °C. Tests in the lab resulted in a maximum heat-sink temperature of 47.8 °C while switching at 15 amps.

FET REVERSE CURRENT

Testing was done on the bottom FET when current is flowing through it in the reverse direction. The normal current path is through the intrinsic diode. However it was observed that when the current is less than 12 amps a lower voltage drop occurs if you turn the gate of the FET on. Reverse current can be forced to flow in the FET, bypassing the intrinsic diode and reducing the voltage drop. Lower switching losses can be obtained during this cycle of operation.

NOISE GENERATION

The switching supply generates noise by nature of the operation. During switching when the top FET turns on, a large current shoots through the top and bottom FET until the intrinsic diode shuts off. When operating at 15 amps output current, this shoot through current is on the order of 50 amps with a duration of 200ns. In order to keep the noise radiated to a minimum the power section was shielded separate from the rest of the power supply. The authors are aware of more elaborate schemes of putting a fast recovery diode in series and another in parallel with the bottom FET. The disadvantage is power dissipated in the series diode making the total losses greater.

The other large items in the power section sheilded were the chokes and caps which make up a Praeg filter [1]. The design specification stated that the 30 kHz 150 volt output switching signal must be reduced to 1 volt RMS at the supply output terminals. This requires a filter with 40 dB per decade roll-off and a break frequency of 1 kHz. The filter chokes selected had an inductance of 500 μH.

FET DRIVERS

The power section uses opto coupled devices to send ON/OFF signals to the FET driver. The driver uses a commercially available device that has it own isolation scheme for the top FET drive. The top FET drive energy

is developed by a bootstrap circuit. The proper use of this device requires the designer to pay strict attention to input gating and minimum pulse widths. It was observed that if a signal less than 50 ns to the lower gate drive, the chip will lock up until it receives another pulse. To ensure lock-up will not occur, the gate logic circuits were designed to produce a minimum pulse of 200 ns.

CONTROL LOOPS

The voltage loop feedback is taken on the H-Bridge side of the the Praeg filters. This signal is edge filtered using an RC time constant of 10μs. A differential amplifier is used to subtract the 2 output legs, and feed an error amplifier that compares the output voltage and the current loop output. The error signal is then integrated to generate a signal that controls the ON time of the top FET from 200 ns to 31.7μs (95% of total time). The voltage loop also determines the direction control, which determines if the output voltage is negative or positive.

The current loop is outside the voltage loop and uses a 50 amp LEM current head for isolated feedback. The LEM is sensitive to external magnetic fields and dv/dt signals on the wire. The head was moved to the front of the 23 inch chassis to remove it from the power section, and reduce magnetic pickup. Early testing was done using differential amplifiers and current shunts. However, these scheme had serious common mode problems at frequencies above 500Hz.

The current loop reference goes through a slew rate limiter (SRL) set to 75 amps per second. The SRL smooths out the steps in the output of a D/A reference card which keeps the power generated in the damping resistor in the filter to a reasonable value. The compensation parameters for the current loop are set up for 5 different load settings ranging from a L/R ratio of 0.95/5 to 0.030/2. The closed loop frequency response for the 1 Henry magnet is 250 Hz. All other magnets have a 300 Hz bandwidth.

PROTECTION & MONITORS

The supply has several internal interlocks that force the supply into the inhibit mode. These signals are dc overcurrent, RMS current, ground fault current, heat sink temp, filter temp, and external permit. The unit also has alarms for low input supply voltage and tracking error. All these faults and alarms are sent to the control system as digital status.

The analog monitors are the program reference, output current, output voltage, RMS current, and current error x100. All the analog signals except the last one are sent to the control system.

Each supply is isolated from the main DC power supply by a 25 amp circuit breaker. Each magnet load has a MOV installed at the power terminals to absorb the inductive stored energy under fault conditions, such as cables being unplugged or power supply failures.

SIZE & AIR FLOW

The units are air cooled and measure 5.25”H x 4.188”W x 23”D.. A total of 4 units are mounted side by side in a standard 19” relay rack crate. A group of 16 supplies will be mounted 4 wide by 4 high. A fan pack will be used to blow air up through the group of 16.

CONTROL POWER

The supplies use +/- 15V, and +5V in each regulator. This power is daisy chained at each unit and comes from a common distribution supply.

MAIN DC POWER SUPPLY

The main supply is designed to provide 180 VDC power to 48 units. This supply consists of a 3 phase transformer with a 480 volt input, a 3 phase full wave bridge rectifier, and a passive filter. The nominal current from the 48 units is estimated to be 120 amps.

PROJECT STATUS

Several prototypes have been operating since last October. Currently 24 units are being built for extended testing in a Main Injector Service Building. After a satisfactory run, any necessary changes will be made and the total quantity needed (275) made to print.

REFERENCES

[1] Praeg, W., A High Current Low Pass Filter For Magnet Power Supplies, pp 16-22,IEEE Transactions On Industrial Electronics and Control Instrumentation, Volume IECI-17, Number1, February, 1970