STRATEGY FOR DEVELOPING FAST BUNCH FEEDBACK SYSTEMS FOR KEKB

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Abstract

KEKB, an asymmetric collider project for the B-physics, is now under construction at KEK Japan. In order to overcome the problem due to expected coupled bunch instabilities, we are developing bunch feedback systems. In these feedback systems we will use signal process systems based on the simple 2-tap filters. The fabrication of the prototype of the signal process board has completed and it worked well in the feedback experiments performed in AR at KEK.

1 INTRODUCTION

Recently, many storage rings which store very high current are in operation or under construction. In these rings, coupled bunch instabilities can be a serious problem in their operation. Several sources, such as cavity impedance, finite conductivity of the beampipe, some ion/electron cloud, $\cdots$ can cause these instabilities. One way to cure them is the use of bunch feedback systems that can treat multiple bunches. However, it is not a easy way to design such feedback systems, because the number of bunches is very large and, consequently, the bunch interval should become very short in these machines.

KEKB, which is an asymmetric e^+e^- collider for B-physics, is one example of such machines. In KEKB, about 5000 bunches/ring (harmonic # is 5120) are stored in the ring of 3019 meters in circumference and the bunch spacing is only 60cm. For several years, we have been developing bunch feedback systems which meet these severe conditions. At present, design of major hardware parts has completed and we have just started to integrate them to a system.

At this stage, discussions with the people who are developing similar feedback systems are very fruitful. For example, in PEP-II[1] and DAΦNE[2], they are developing the same kind of feedback systems. Since these feedback systems must satisfy a number of tight conditions, the hardware that satisfy them can not have wide variety. In fact, the front-end circuit for the bunch-position detection is more or less similar among these three examples. But we can find several differences in some hardware schemes as summarized in the table below.

	KEKB	PEP-II	DAΦNE
L. kicker	d.tube/cavity	d.tube	cavity
electronics	hard-base	soft-base	soft-base

The first example of the differences is the design of the longitudinal kicker. For PEP-II, they will use the drift-tube type of kickers[3] that is very wide-banded. These kickers have already been installed in APS at LBNL and they successfully damp the longitudinal oscillation. In DAΦNE, they are developing a very low-Q cavity[4] which has higher shunt impedance than the drift tube kicker. The second example of the difference in hardware scheme is the signal process system. Even though it is common to all of them to use the digital technology, there are some differences. In PEP-II and DAΦNE, the signal processing in the longitudinal plane is done with a system based on Digital Signal Processors (DSP). Since this system is programmable, it is very flexible. In KEKB, on the other hand, we will not use the DSPs but use hardware-based systems. In this paper, we describe our basic strategy of developing the feedback systems particularly paying attention to this signal processing system.

2 SIGNAL PROCESSING OF THE KEKB SYSTEM

2.1 Basic idea - 2-tap digital filters

The basic idea in designing our signal process system is to use the concept of the 2-tap digital filter. Since we closely discussed the features of the 2-tap digital filter in other papers[5][6], we briefly review its characteristics. In many feedback systems, the feedback-kick is given to a bunch after the phase of the betatron (or synchrotron) oscillation is rotated by the angle $\pi/2$ (mod 2π). Inspired by this usual method, we recognize that it is possible to damp the oscillation by kicking the bunch after the phase is rotated by $3\pi/2$. But, in this case, the sign (=direction) of the kick should be inverted; otherwise, it becomes an exciter not a damper. The idea proposed by F. Pedersen[7] is to combine two feedback loops in parallel; one is of $\pi/2$-delay the other is of $3\pi/2$ delay with the inverted sign. It is very advantageous for us to use this combining method because it can work as a DC-cut filter. Naturally, we need not prepare two feedback systems for these two cases actually. The combination can be realized by a simple subtract operation performed in digital components.

2.2 Outline of the design

Guided by our basic idea explained above, we made a conceptual design of the signal process system. Considering very simple algorithm of the 2-tap filter we judged it to be reasonable to make this logic by hardware. This choice enables us to construct a very fast processing system, i.e. a bunch-by-bunch signal processing with the bunch frequency of 500MHz is feasible with this system.

At the practical design stage, we found that

- it will be advantageous to fabricate a de-multiplexer which can reduce the signal rate of 500MHz to easy-

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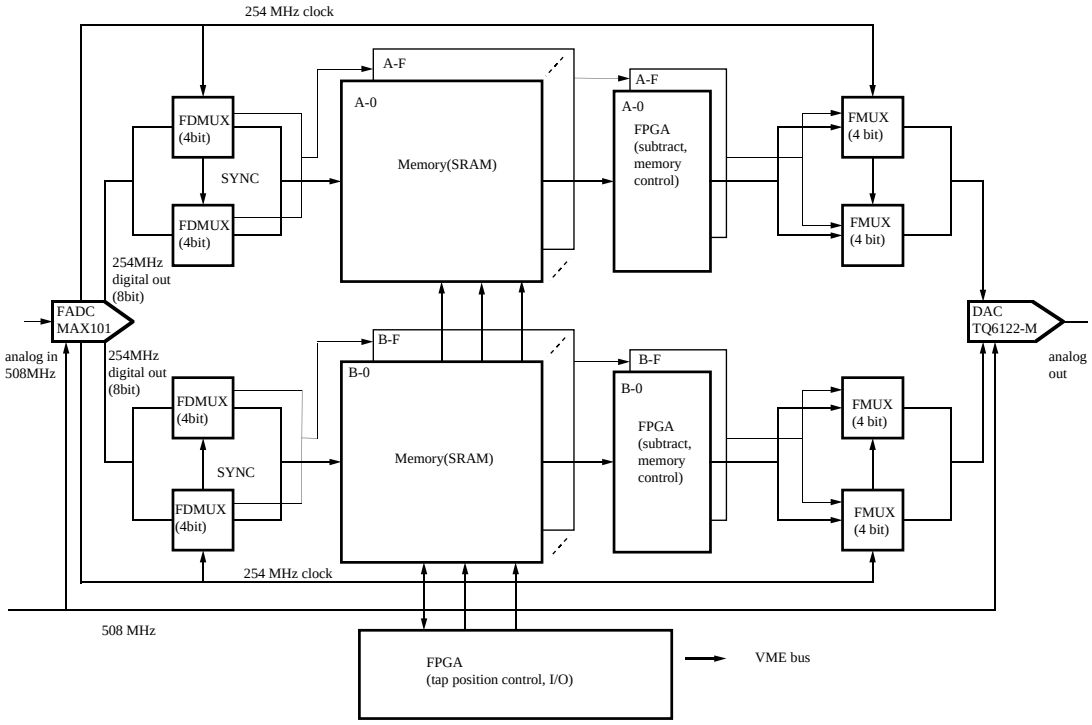

Figure 1: Block diagram of the signal process board. The output of the ADC is fed into the de-multiplexer fabricated as a custom LSI (FDMUX). It reduces the signal rate from 254 MHz to its 1/16. The output of the 2-tap filter, which is made up with the memory and the FPGAs, is fed into the multiplexer (FMUX) that is the counter-part of FDMUX.

manageable frequencies. It can be realized Ga-As LSI chips. Since we were not able to find such LSI commercially, we decided to fabricate it as a custom LSI as well as its counter-part, the high speed multiplexer.

- A set of circuitry for one plane can be packed in only one board, even though it treats 5120 bunches by using the de-multiplexer. The size of the board is almost the same as that of the 3-height VME board.

A block diagram of this signal process board is given in Figure 1. As we described this system in other paper[8] in detail, here we explain it very briefly. The board has an A-to-D converter for the input, two arrays of memory chips with subtract logics and a D-to-A converter for the output. The interface between the ADC and the memory is a pair of the FDMUXs. The 2-tap filter scheme is realized by these two arrays of memory and the subtract logic. The length of the memory is 1 Mbyts/array. A pair of FMUXs interfaces output of the filter and the DAC. The board itself has a non-standard size, but it is equipped with a VME interface. The tap positions of the 2-tap filter are easily set through this interface. Additionally, the content of the memory can be read out also through this VME interface when the system is at "not running" status.

2.3 Evaluation of this scheme

In our hardware-based scheme, we can stuff a large portion of the technical difficulties due to the high-speed into the custom LSIs. They can reduce the signal rate from roughly 500MHz (in our practical application we use 254 MHz of the input signal) to its 1/16, and vice versa. Then, outside of the LSIs, almost all the signal transportation is in only 16 MHz. The cost of the fabrication of these LSIs is a little expensive but thanks to this custom LSI, we can construct very fast devices without serious difficulties. This can be one of the strategies of making a system when the number of within-laboratory staffs is considerably limited. The high cost of these LSIs is paid by following two facts,

- The 2-tap signal process board can be commonly applicable to the longitudinal and transverse systems. If we used a slower system, it might not be usable for the transverse systems.
- By slightly changing the design, we can make a very powerful memory systems as explained in the next section. There must be many potential applications of this memory system.

3 THE MEMORY BOARD

3.1 Design of the memory board

If we remove the output part (FMUXs and the DAC) from our 2-tap filter board and add more memory chips in place of it, the board becomes a very fast, large-size transition memory system. We call it "the memory board". It has the common mother board with the 2-tap signal process board. The amount of the memory is increased from 1 Mbytes to 20Mbytes. This can store the history of oscillation of 5120 bunches over 4096 turns.

3.2 *Application of the board*

There are a wide range of the applications of this memory board. Several examples are a bunch-by-bunch current monitor and a bunch by bunch tune meter. The 4096 turns of data of oscillation is sufficient enough to determine the tune.

Another application of the memory board is to store the time-domain data of oscillations of many bunches. It should be a powerful tool for studying the behavior of bunches under mulitubunch operation. We are planning to use this system in the photo-electron instability experiments to be performed at BEPC in Beijing, China[9].

4 PRESENT STATUS

4.1 *The 2-tap filter board*

In the last autumn the first version of the 2-tap signal-process board completed. By using this board and other components, we have performed feedback experiments in AR at KEK. A detailed description of these experiments is given in another paper in these proceedings[10]. In these experiments we were successfully damped the longitudinal oscillation with the 2-tap filter board.

What we must describe here is a function of the 2-tap filter board as a medium-size transient memory. As explained above, it has 1Mbytes of the memory. That can record behaviors of bunches over 1600 turns when the number of bunch is 640, where 640 is the harmonic number of AR. Utilizing this function, we were able to perform several experiments of accelerator physics. The preliminary reports of these experiments are given in these proceedings[11][12].

4.2 *The memory board*

The fabrication of first prototype of the memory board has completed just after the experiments in AR. It will be exported to China this summer for the experiments at BEPC.

5 FUTURE PLANS

According to the general schedule of KEKB, the commissioning of LER will be started at the middle of next year. Until this time, we must carry out the following things:

- fabrication of the DAΦNE-type kickers
- development of the control software

5.1 *The longitudinal kicker*

We made the feedback experiments in AR with the drift-tube type of the longitudinal kicker. The experimentally-estimated shunt impedance is consistent with the calculation[13]. In this sense, the experiment was successful. But we still hope higher shunt impedance because the reduction of the number of the kickers as well as that of power amplifiers is seriously desired for practical and economical reasons. The cost for these amplifiers will take a large part of the total budget for the feedback systems.

Then we next try to construct the DAΦNE type kickers whose estimated shunt impedance is about twice of the drift-tube kicker of 2-inner electrodes. The operating frequency of the kicker in KEKB is very close to that in DAΦNE. Then the kicker will be usable with small correction in the design.

5.2 *The control software*

The accelerator control system of KEKB is based on EPICS[14], in which hard-ware accesses are done through VME computers. As described above, our signal process board and the memory board have the VME interface. Since these boards are “user-made” we must code the “device support” for practical operation. Particularly, it is essential to write a flexible support program for the memory board, because it will be used for various purposes.

6 SUMMARY

We fabricated the signal process systems for our bunch feedback systems. This system is based on hardware logic and can work at the bunch frequency of 509MHz. One of the main features of system is that we developed a custom LSI for fast de-multiplexing and multiplexing. The fabrication of these custom LSI is a little expensive. But thanks to these LSIs, we can made not only the feedback electronics but also a powerful transition memory board. It can be a powerful tool for the beam diagnostics.

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