FAST FPGA BASED LOW-TRIGGER-JITTER WAVEFORM GENERATOR METHOD FOR BARRIER-BUCKET ELECTRONICS AT FAIR*

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Abstract

A new method for low trigger-jitter waveform generation is presented. The targeted application is the time-delayed, trigger synchronous waveform generation. The method can be implemented on a single FPGA, which drives an ADC. The phase-jitter between a trigger signal fed to the FPGA and the generated single sine waveform is σ= 40 ps and 275 ps peak-to-peak. The response time of the wave form generator is 50 ns. The amplitude and the offset of each sine wave can also be manipulated in real time. The waveform generator was designed for the use in the Barrier-Bucket system of the SIS100 synchrotron at the new Facility for Antiproton and Ion Research (FAIR) in Darmstadt, Germany.

INTRODUCTION

The GSI Helmholtz Centre for Heavy Ion Research in Darmstadt, Germany is an accelerator facility for High Energy Physics (HEP) research. In collaboration with 16 countries and physicists from all over the world, the Facility for Antiproton and Ion Research (FAIR) will be built as a major extension of the existing facility and will be one of the largest accelerator facilities in the world.

The presented waveform generator method is designed for the use in the pre-compression stage of the new SIS100 synchrotron. The existing SIS18 will be used as booster and will inject bunches of particles into 8 of 10 SIS100 buckets. After the particles have been accelerated to the final speed in the SIS100, they have to be compressed to a single bunch that takes 1/3 of the circumference. The preferred method to perform this task is called Barrier-Bucket. In this method, the amplitude of the bucket forming sine waves, which hold the bunches, is decreased adiabatically. After a certain time the bunches merge into a single long particle bunch in between the remaining sine waves. Now, to compress the beam without the loss of particles, one wave has to be moved towards the other adiabatically, means in steps less than 1 ns. Both sine waves have to be generated synchronously to the revolution trigger, coming from the Central Control System, which controls also the amplitude and the voltage offset of the sine waves. The BB-method is illustrated in Fig. 1. The constraints for the waveform generation system, listed in Table 1, are given by the physics of the accelerator and the desired bunch quality.

The task is therefore to gain control over the phase of the generated single sine waves in the sub nano-second region with a low response time. For this purpose a new waveform generation method was developed and implemented.

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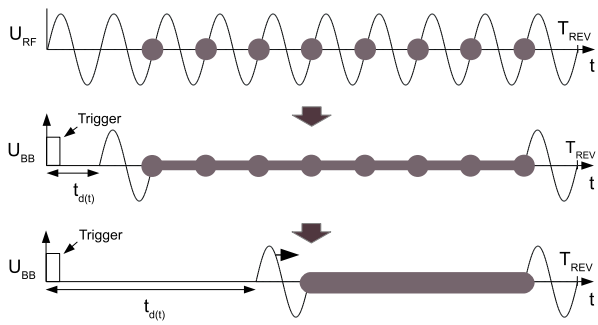

Figure 1: The procedure for beam pre-compression with the Barrier Bucket method (simplified).

Table 1: Specifications for the Barrier-Bucket Low-Level RF-System

Parameter	Value
Barrier Frequency f_b	1.5 $\pm$ 0.2 MHz
Revolution Period T_{REV} (= Trigger Period)	9.1 to 3.7 μs
Moving Time T_{MOV}	10 to 200 ms
Moving Step Resolution $\Delta t_{d(t)}$	$\leq$ 1ns
BB signal rise/fall time t_R and t_F	$\leq$ 10ns

We will introduce the new method in the next section. In the section "Design" the design structure and operation are explained. Subsequently, the measured performance of the system will be presented, followed by a conclusion.

WAVE GENERATION METHOD

In existing asynchronous triggered DDS methods, the incoming trigger signal is sampled with the internal system-clock frequency f_{sys}. As soon as a 0/1 transition is detected, a Digital-Analog-Converter (DAC) is driven by the system-clock and fed with the grid points of the desired waveform. The standard deviation of the resulting trigger-waveform jitter equals then $1/(f_{sys} \cdot \sqrt{12})$. To overcome this limitation, additional effort is necessary on both sides - on the input processing as well as on the signal synthesis part. The given task can therefore be divided into two subtasks. First, the relation of the incoming trigger-signal phase to the system-clock signal phase $\Delta\Phi$ has to be determined with a higher precision than simply by sampling the trigger signal and second, the generation of the phase accurate sine wave using this information. This procedure is illustrated in Fig. 2. In the following sections, the methods for a high precision phase measurement and for phase accurate signal generation are introduced.

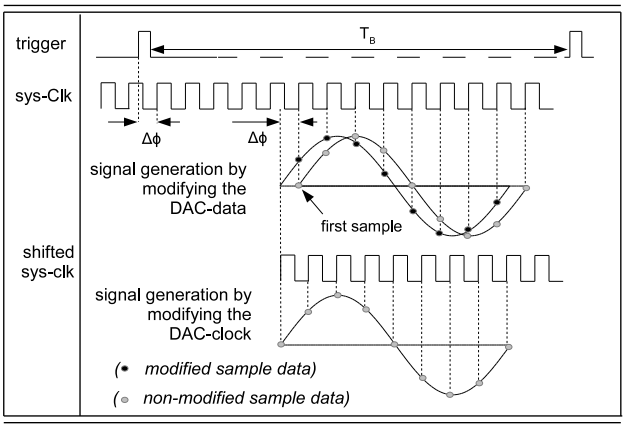

Figure 2: Principle of the phase accurate waveform generation by modifying the DAC data or, alternative, the DAC clock.

Phase Measurement

The first step in generating a low trigger-jitter waveform is the measurement of the phase relation between the trigger signal and the system clock, since the system clock is then used for the DDS algorithm. This corresponds to a time interval measurement. The accuracy has to be as good as possible, because the maximum phase deviation in the whole method is increased by the maximum deviation of the phase measurement. Therefore, to reduce the portion of the measurement inaccuracy, a high-precision FPGA time-to-digital (TDC) method was used for this purpose, which ensures a maximum deviation down to ∼30 ps [1]. The used TDC method is a tapped delay lines (TDL) technique with enhanced accuracy. The details of this TDC design can be found in [1].

Phase Accurate Waveform Generation

Generally, there are already methods for the generation of phase shifted waveforms. For example the CORDIC algorithm can be used to generate waveforms with the desired phase-offset by starting with a certain amplitude offset as is shown in Fig. 2. This approach works well for generation of continuous signals, when the waveform at the beginning and at the end of the waveform is of no interest. If a well shaped single sine wave has to be generated, one has to consider the phase-offset-cut artifacts on the edges of the waveform due to the variable phase offset, which results in large phase-jitter on the sine wave edges. A good alternative avoiding these effects is the shifting of the ADC driving clock instead of the ADC data as is shown in Fig. 2.

The common method to perform phase-shifts of the system clock in FPGA is using the build-in Phase-Locked-Loop (PLL) or a Delay Locked Loop (DLL). Here a phase-shift granularity of $(1/1024) \cdot T_{sys}$ is available [2]. The disadvantage of this approach is the relatively large reconfiguration time of the PLL that can take several microseconds [2]. These parameters exceeded the given constraints of our application. Therefore, a new method for the generation of a phase-shifted clock signal was implemented on a Virtex-4 FPGA. The implemented "phase-shifter" uses the routing resources of the FPGA as delay elements and produces delayed versions of the system clock. This is done by deploying the carry-chain MUX resources to access the clock signal. As the carry multiplexer are arranged in a column an evenly delayed signal can be produced in steps of 100 and 200 ps. The switching is performed within one clock cycle - means: down to 2 ns response time on the current FPGA families [3].

DESIGN

Structure

For the implementation of the waveform generator we take a phase-shifter, a high-precision TDC for phase-relation measurements, two secondary FPGA-TDC to measure phase-shifter delays and the DDS building block, which feeds a 14-bit ADC outside the FPGA. As the shifter delays measurements can be repeated, the secondary TDCs have a lower resolution and need less resources. We deploy the design from [4] for this purpose.

The implemented design makes extensive use of the temperature and voltage dependent gate delays in the FPGA. Therefore additional effort is needed to ensure a stable operation [4]. For this purpose a calibration and continuous recalibration functionality has been implemented on-chip for the phase-shifter delays as well as for the TDCs. The used calibration methodology can be found in [5]. The (re)calibration of these elements is scheduled within the idle phases of each element between the incoming trigger events. Since the trigger frequency may not be sufficient for using the trigger input for calibration, a controllable, system clock uncorrelated, internal pulser was implemented, which can be used as calibration signal.

The coarse structure of the system is shown in Figure 3. Its operation will be described in the next section.

Operation

The first task in the initialization phase of the system is the calibration of the TDCs. The inputs of the three TDCs are switched to the internal pulser and the 2^{16} events for the first calibration are collected. After the shifter TDCs are calibrated, the resulting delay of each shifter position is measured. Using this information the SD-LUT is constructed, which maps each possible needed delay within the system clock period (T_{SYS}) to a shifter position. After these steps the system is fully operational. Before each trigger event, the system receives three optical information streams - two streams containing the amplitude and amplitude offset information and one with the current phase-offset. When a trigger signal arrives, the time interval between the rising edge of the trigger and the following rising edge of the system clock is measured with the high-precision TDC. From this measurement and the current phase offset the required shifter delay is calculated in the event-phase-logic. A coarse counter is then loaded with the coarse portion of the phase-offset, which has a granularity

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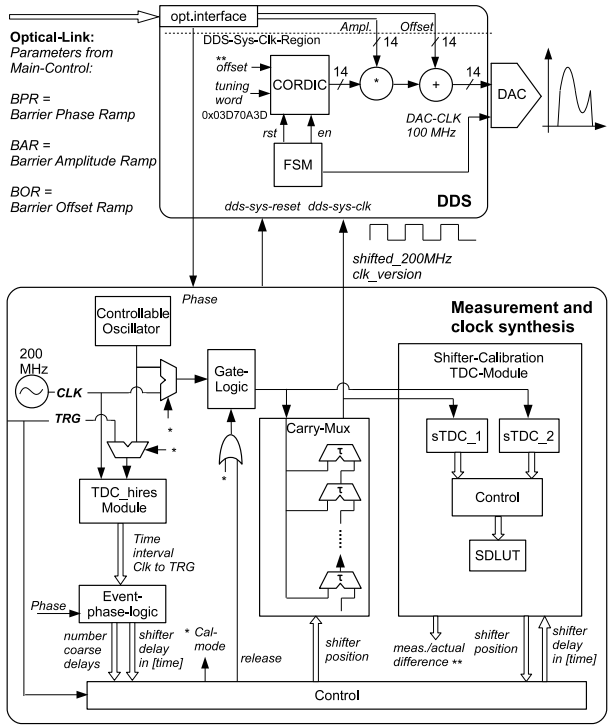

Figure 3: The block diagram of the system. The additional path for the combined mode is marked with (**).

of T_{SYS} and the phase-shifter is switched to the position corresponding to the fine shift value.

All these steps are done within a constant time window, which finishes with the release of the back-running coarse counter. As soon as the counter value reaches zero, the clock gate at the phase-shifter input is released and a defined number of shifted system clock pulses is generated. This pulse train is used as clock signal for the DDS part of the system. There, a finite state machine generates the DAC clock and the corresponding sine grid points by driving a CORDIC unit. At this point, the DAC data values can be manipulated, to adjust the needed sine amplitude and sine offset.

To further improve the jitter characteristics the combination of DAC data and DAC clock manipulation can be applied. For this purpose the difference between the actual delay of the set shifter position and the measurement value is sent to the DDS part of the system to adjust a corresponding offset in the DAC data.

MEASUREMENTS

Although the whole system can be implemented in a single FPGA connected to a DAC, the current setup is distributed between two FPGA boards, featuring together the needed interfaces. The clock pulse train is fed into the DDS-System by a single ended connection and is therefore exposed to the electromagnetic noise. For this reason the achieved performance was characterized by measuring the trigger-jitter of the generated pulse-train, the sine wave generated by DAC clock manipulation only and the sine wave generated by the combined method. The measured trigger-jitter of the pulse-train is σ = 58 ps and 350 ps peak-to-peak. The phase-jitter of the basic/combined method is σ= 63/35 ps standard deviation and 500/270 ps peak-to-peak deviation. Hence, the achievable performance for a single FPGA implementation is $\sigma = \sqrt{35^2 - (63^2 - 58^2)} \approx 25$ ps. The test readings of the sine wave for the combined method are presented in Fig. 4.

CONCLUSION

A new method for triggered waveform-generation was presented. The method of combined manipulation of the DAC-data and DAC-clock implementable in a single FPGA over-fulfills the requirements nearly by two orders of magnitude and outperforms the known instrumentation in means of trigger-jitter and device costs.

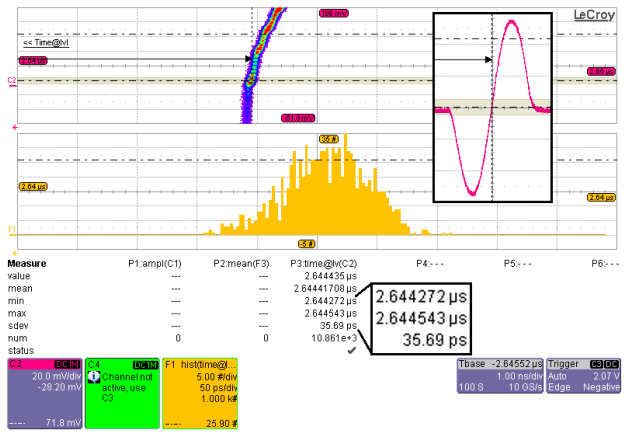

Figure 4: Jitter measurement between the trigger signal and the generated sine wave.

REFERENCES

[1] E. Bayer, P. Zipf and M. Traxler, "A multichannel high-resolution (<5 ps RMS between two channels) Time-to-Digital Converter (TDC) implemented in a field programmable gate array (FPGA)", IEEE NSS/MIC 2011, pp.876-879, 23-29 Oct. 2011.

[2] Xilinx: *Virtex-4 FPGA Configuration User Guide*, UG071 (v1.11) June 9, 2009, downloaded on: http://www.xilinx.com/ support/ documentation/ user_guides/ ug071.pdf.

[3] Xilinx: *Virtex-7 T and XT FPGAs Data Sheet: DC and AC Switching Characteristics*, DS183 (v1.12) March 7, 2013, downloaded on: http://www.xilinx.com/support/ documentation/ data_sheets/ ds183_Virtex_7_Data_Sheet.pdf

[4] E. Bayer, M. Traxler, "A High-Resolution (<10ps RMS) 48-Channel Time-to-Digital Converter (TDC) Implemented in a Field Programmable Gate Array (FPGA)", IEEE Trans. on Nuclear Science, vol.58, no.4, pp.1547-1552, Aug. 2011.

[5] J. Wu, "Several Key Issues on Implementing Delay Line Based TDCs Using FPGAs," , IEEE Trans. on Nuclear Science, vol.57, no.3, pp.1543,1548, June 2010.