CONCEPT AND ARCHITECTURE OF THE RHIC LLRF UPGRADE PLATFORM

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BROOKHAVEN NATIONAL LABORATORY

ACCELERATOR DIVISION

Outline

- Platform Concept
- Architecture
  - Hardware Platform
  - Software (Embedded) Platform
  - System Development
  - System Integration
- Demonstration

RHIC LLRF Upgrade Project

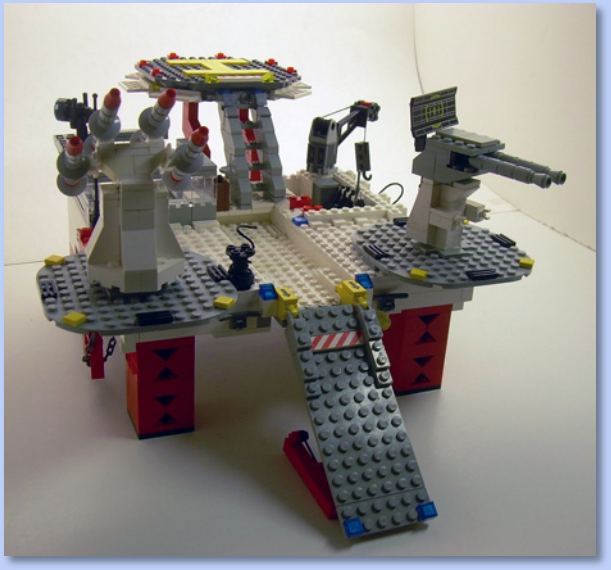
The goal of the RHIC LLRF Upgrade project was to develop a flexible and modular digital LLRF control system which would satisfy the variety of application demands we have.

The desire to develop a system which was generic and modular was the basis for the overall concept ...

It should comprise a platform.

Platform – What Does It Mean?

A base of technologies upon which other technologies or systems are built



LEGO G.I. Joe Transportable Tactical Battle Platform

http://www.hisstank.com/gi-joe-news
http://shop.lego.com

"Lego bricks can be assembled and connected in many ways, to construct such objects as vehicles, buildings, and even working robots."

http://en.wikipedia.org/wiki/Lego

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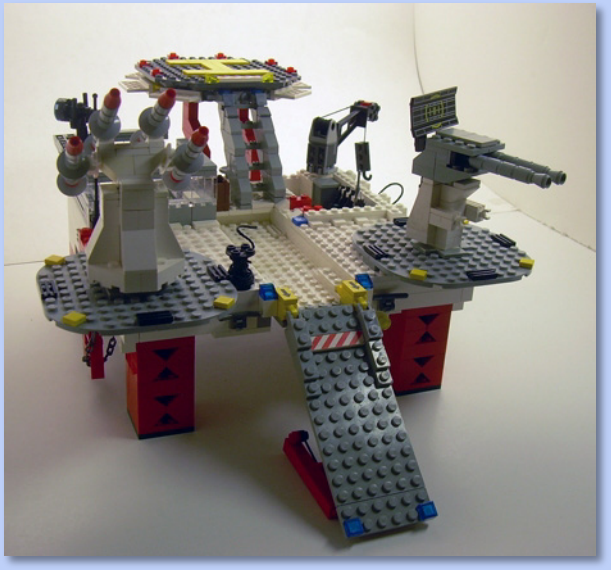

LEGO G.I. Joe Transportable Tactical Battle Platform

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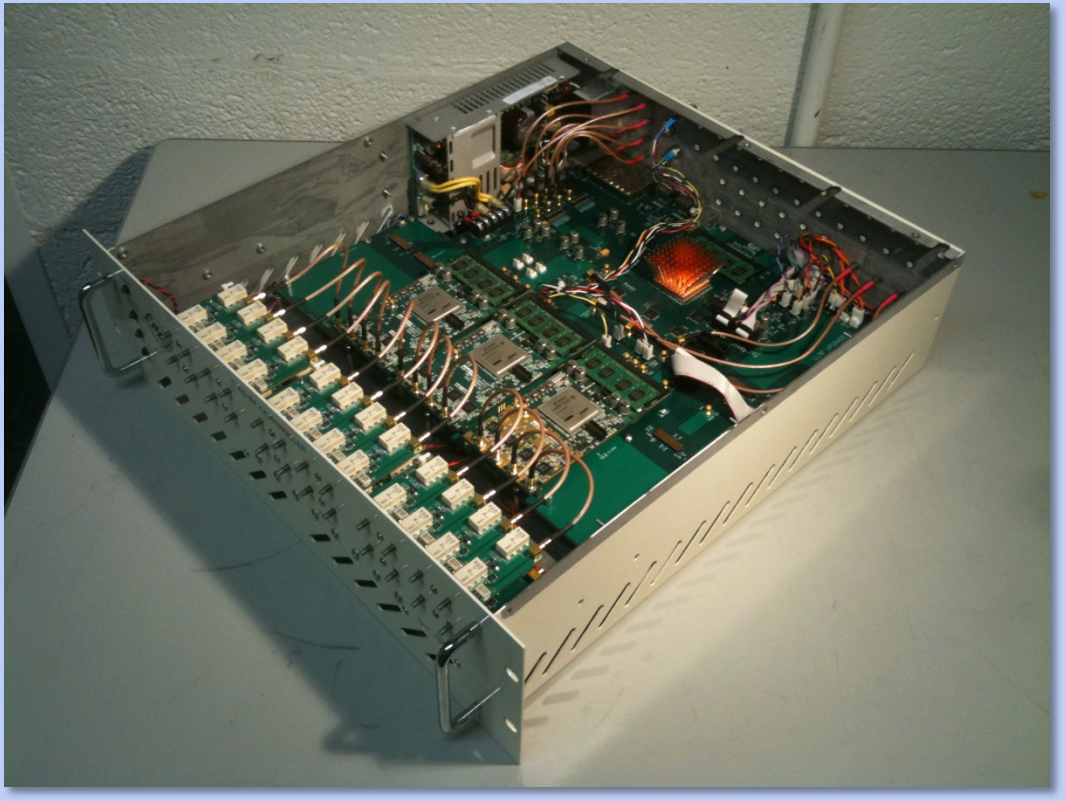
A base of hardware, software and firmware upon which digital signal processing and control systems are built

RHIC LLRF Platform

WEOBN5 - "Concept and Architecture of the RHIC LLRF Upgrade Platform"
MOP283 - "A Hardware Overview of the RHIC LLRF Platform"
MOP296 - "Embedded System Architecture and Capabilities of the RHIC LLRF Platform"
MOP282 - "A Deterministic, Gigabit Serial Timing, Synchronization and Data Link for the RHIC LLRF"

Architecture - Hardware Platform



MOP283 - “A Hardware Overview of the RHIC LLRF Platform”

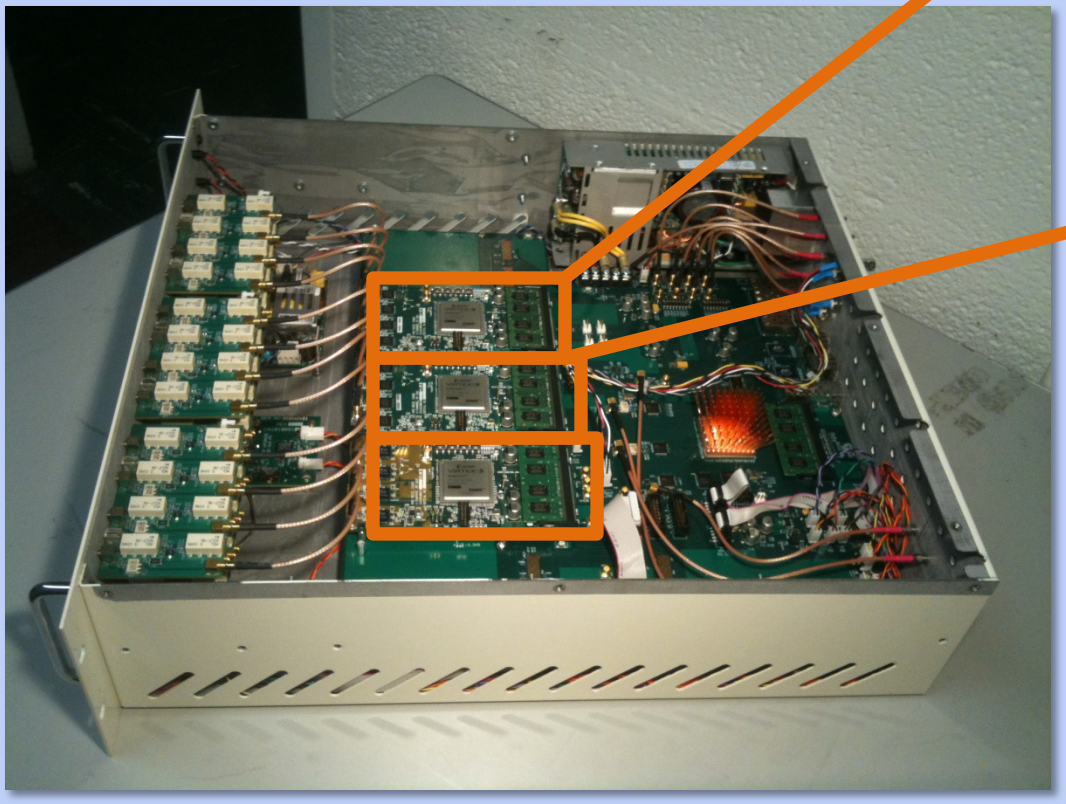
Platform hardware comprises two primary building blocks

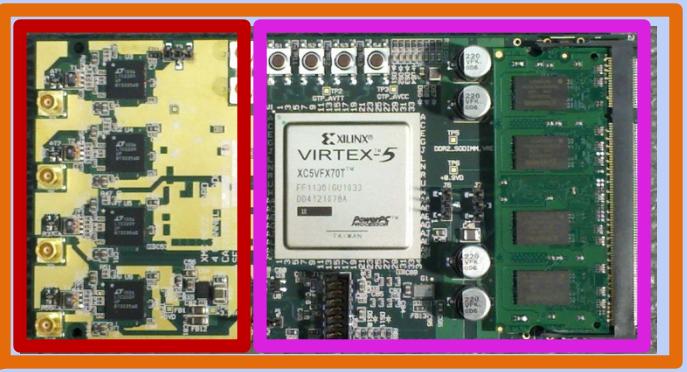
- Carrier Boards
- Daughter Modules

Systems are assembled by combining these in various ways

Hardware Platform – Daughter Modules

Daughter modules provide the application specific functionality for a particular system implementation





MOP283 - "A Hardware Overview of the RHIC LLRF Platform"

MOP203 – "RHIC Spin Flipper AC Dipole Controller"

Currently have 3 modules
- 4 CH Wideband DAC
- 4 CH Wideband ADC
- RHIC Spin Flipper Module

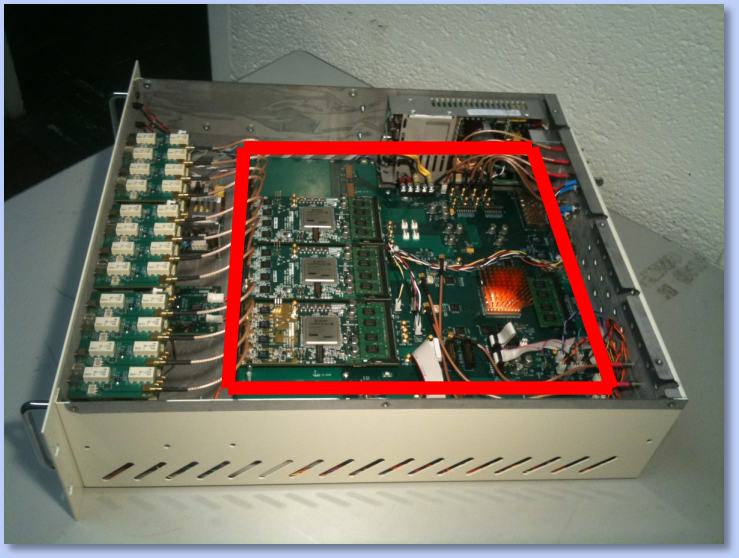
Custom front end design

Common back end design
- Carrier Interface (XMC)
- Peripheral support (DDR2, FLASH, etc.)
- DC Power Supplies

FPGA based (Xilinx Virtex-5)

Hardware Platform – Carrier Board

Carrier Board is the central component of the platform



MOP283 - “A Hardware Overview of the RHIC LLRF Platform”

Hosts up to six daughter modules

Supports internal functionality and external interfacing

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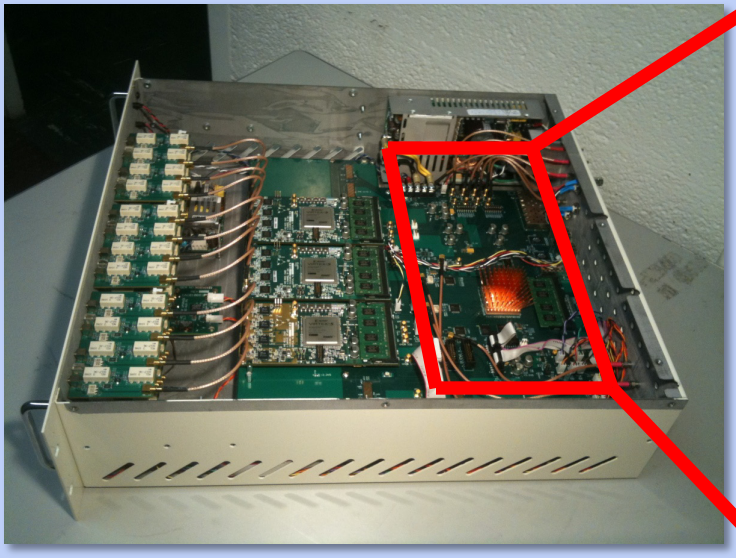

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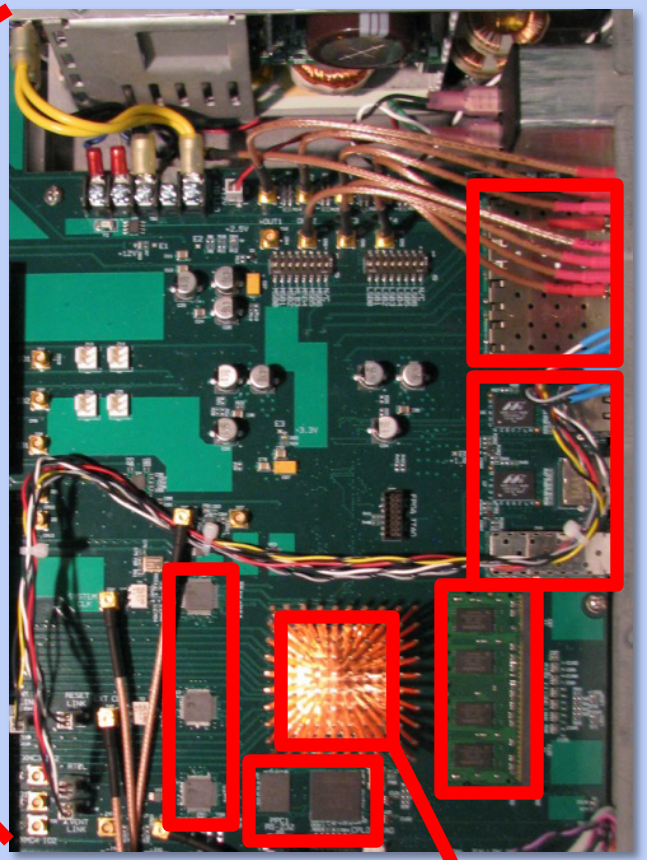

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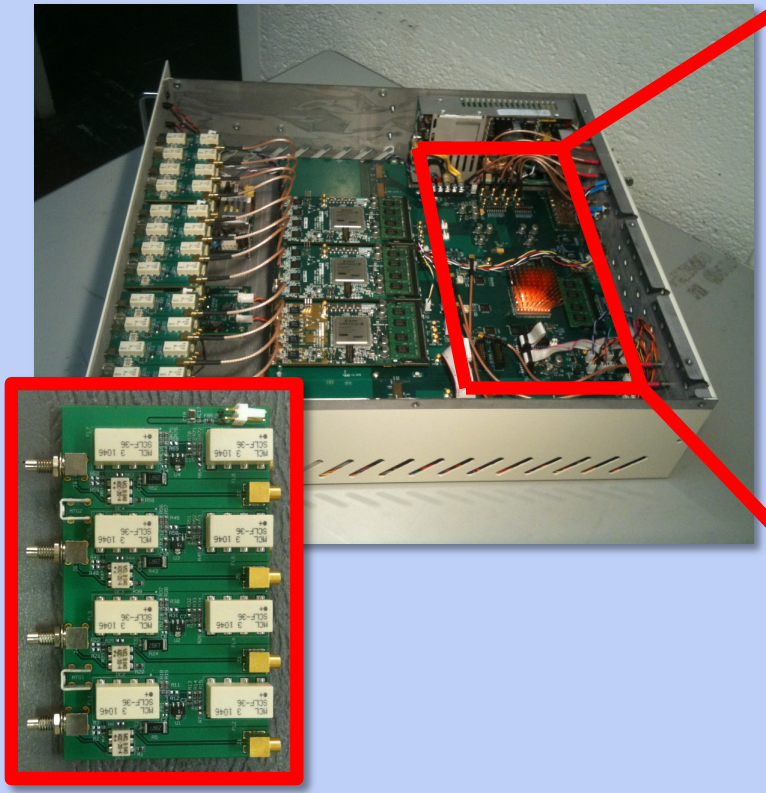
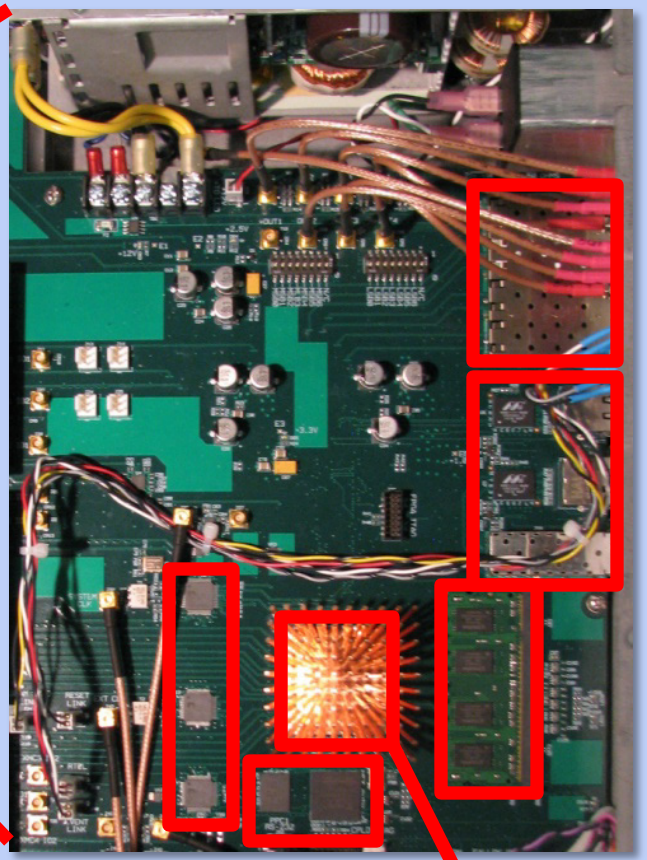


Filtering and buffering separated from daughter modules

System Monitor

DC Power

6x Daughter XMC Mezzanine Interfaces



AC Power

Digital IO

4x Gigabit Serial

2x Gigabit Ethernet

DDR2 SO-DIMM

Low Noise Clock Dist.

FLASH

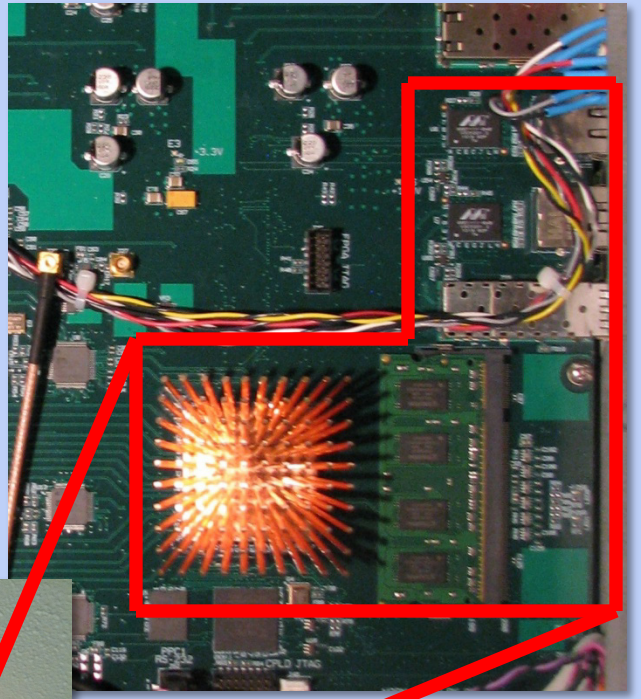
Virtex-5 FPGA

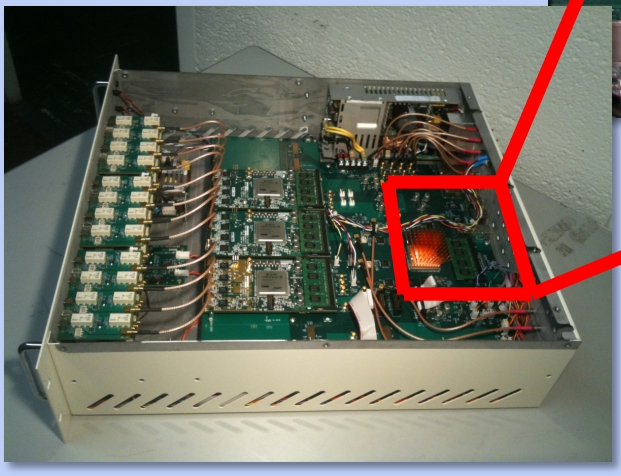
Embedded Platform

Based on an embedded PPC440 processor core inside the Virtex-5 FPGA

Key to the flexibility of the system

MOP296 - “Embedded System Architecture and Capabilities of the RHIC LLRF Platform”





Embedded Platform – Carrier Front End Computer (FEC)

Based on an embedded PPC440 processor core inside the Virtex-5 FPGA

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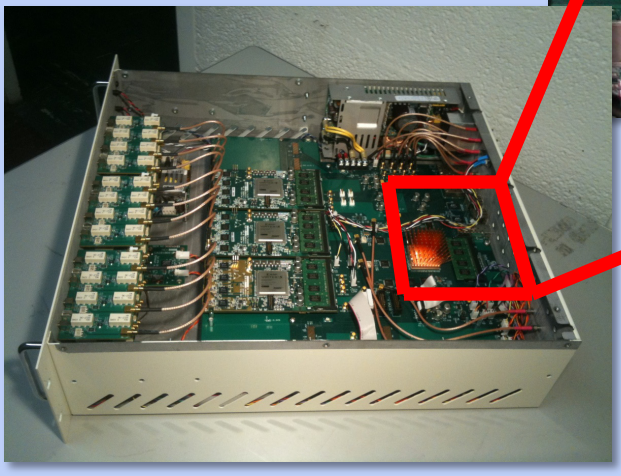
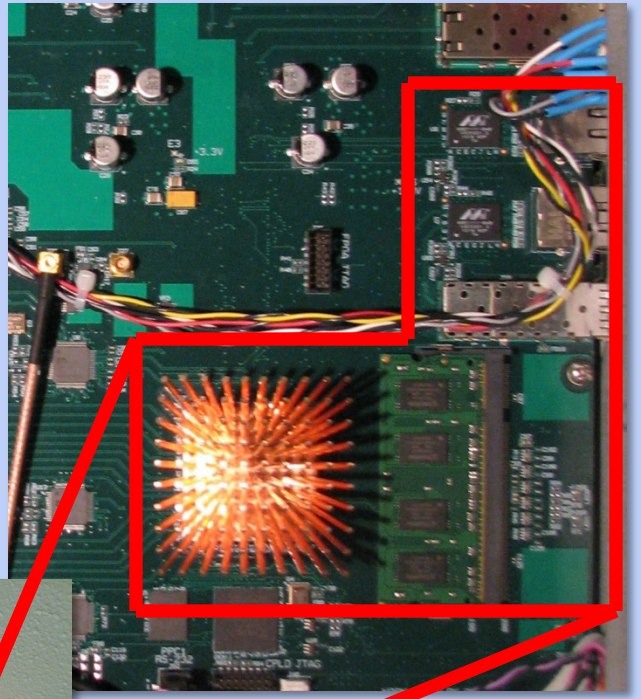




Front End Computer (FEC) – Like an EPICS IOC, the interface between controls network and the accelerator system hardware

FEC implementation is indistinguishable from our older RHIC VME based FECs

Runs VxWorks for RHIC compatibility reasons
- RT Linux or other O/S

Integrated support for standard RHIC Control System Links
- Real Time Data Link (distributed data)
- Event Link (distributed event based timing)

Embedded Platform – Daughter Modules

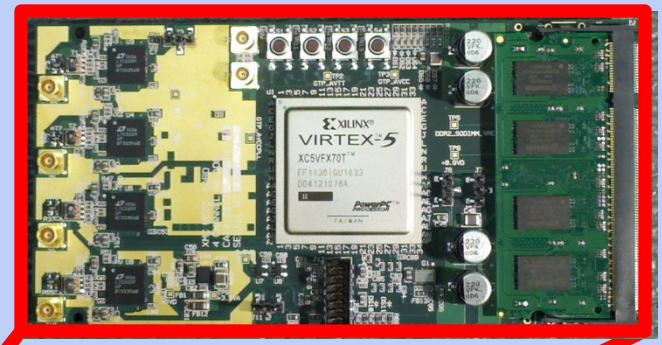
Daughter modules feature the same Virtex-5 FPGA

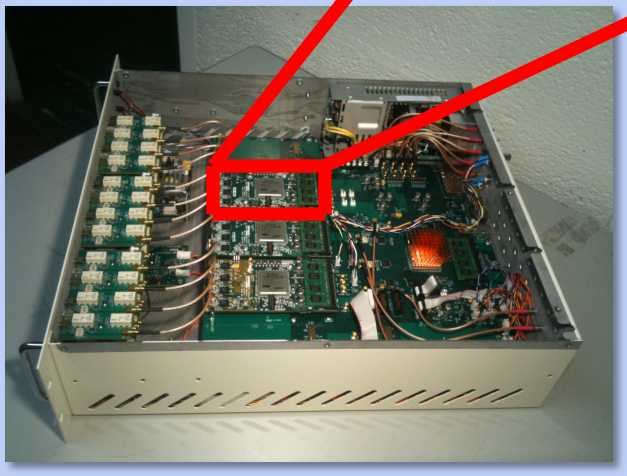
Typically run stand-alone code (No OS)

All designs freely mix FPGA VHDL code and high level code (e.g. C code)

FEC – Daughter Communication
2.5 Gbit/s Aurora links

To the FEC, daughter modules are just another part of their unified memory map

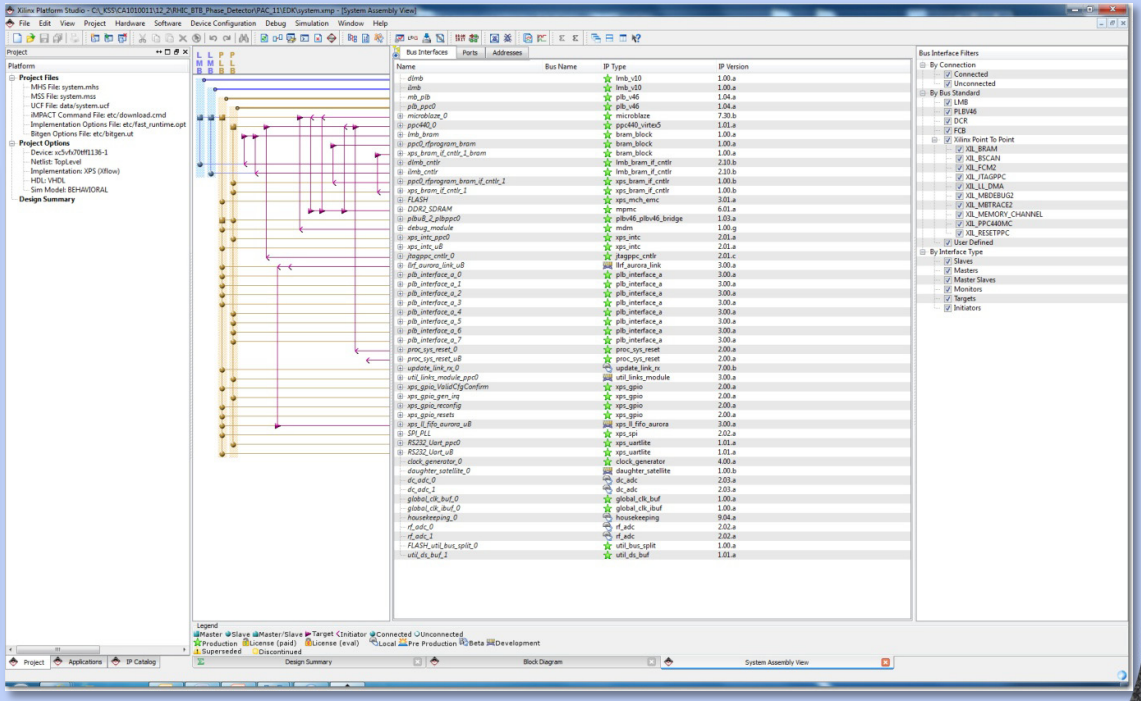




Development for the Platform

Define the FPGA internal system architecture

Build a system by adding and connecting components in a GUI (Xilinx Platform Studio)



Embedded System Development

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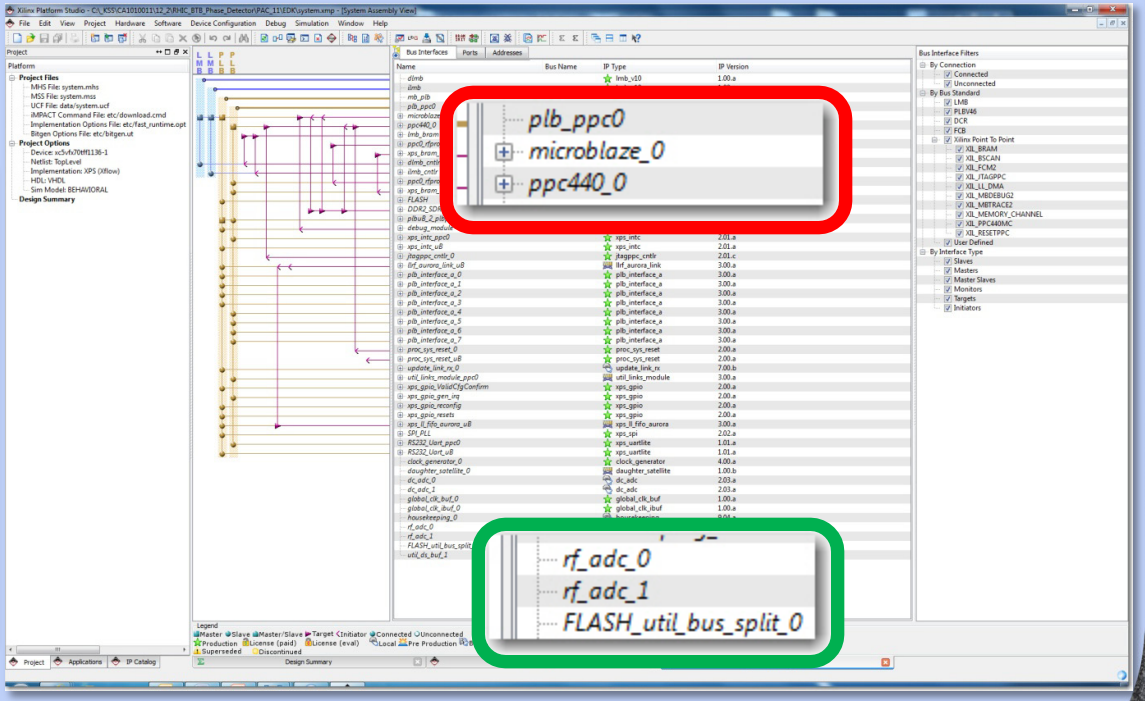
Numerous standard peripherals can be added via drag and drop



Custom components developed when no standard component exists

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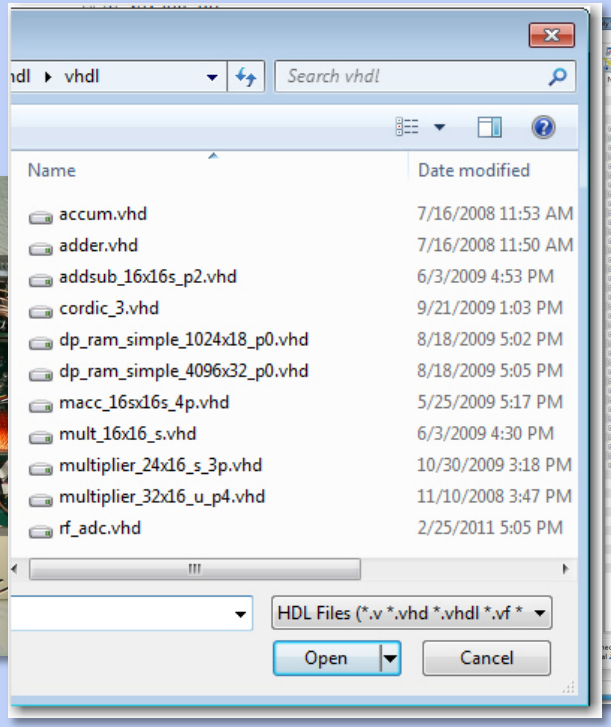
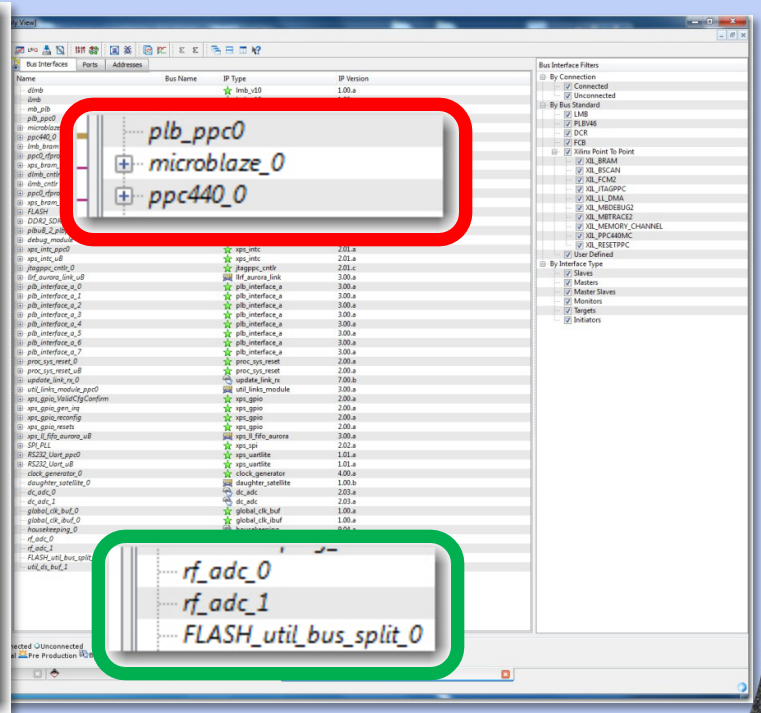




VHDL files for component “rf_adc”

Custom components developed when no standard component exists

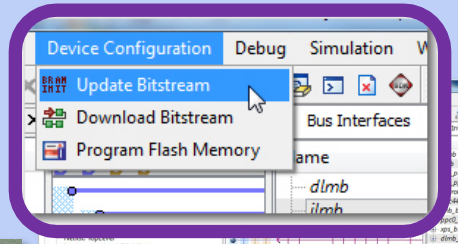
Embedded System Development

Define the FPGA internal system architecture

When done, generate a bit file - the binary program used to configure the FPGA

Remote reconfiguration of any FPGA via Ethernet

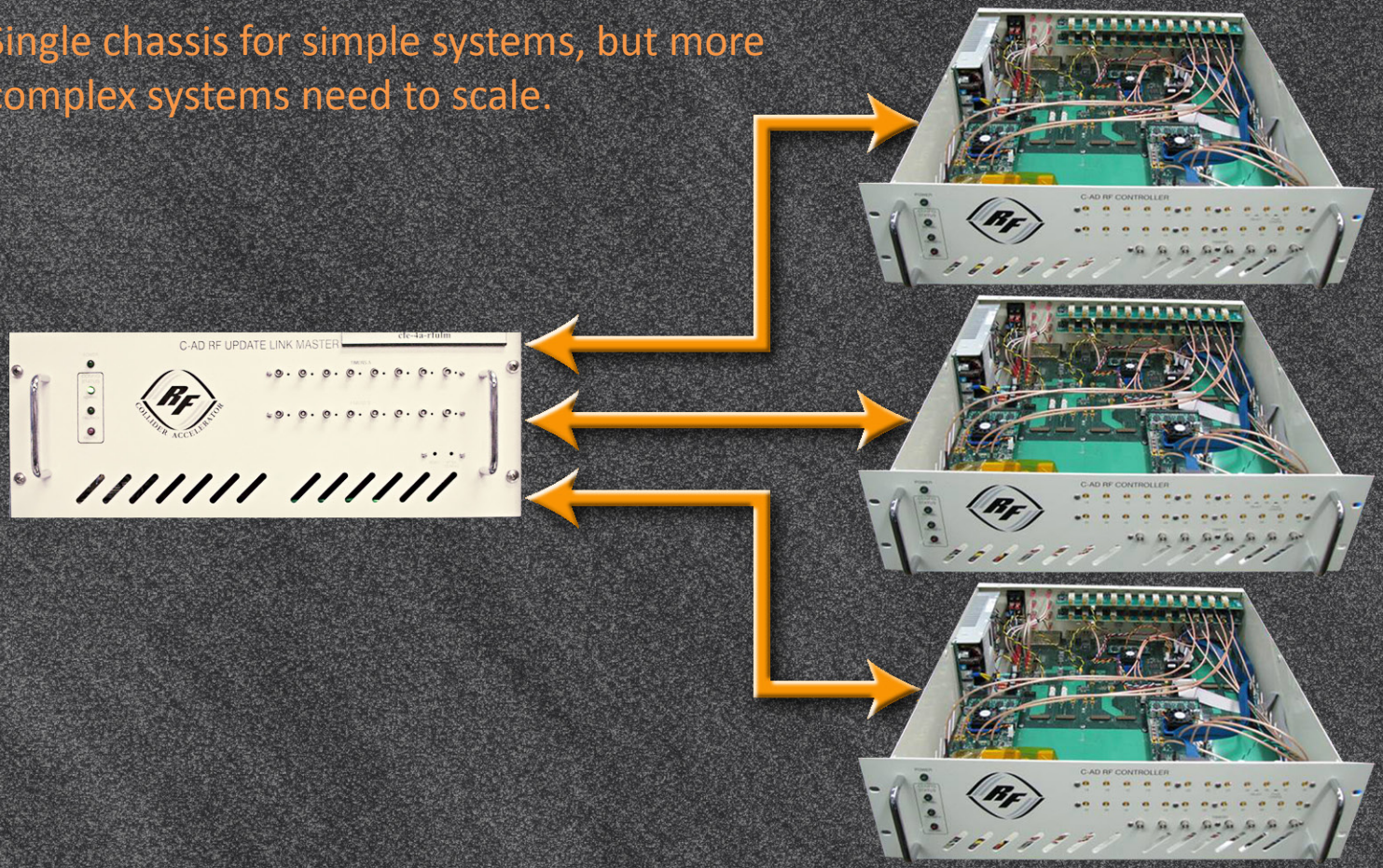
Numerous standard peripherals can be added via drag and drop



Custom components developed when no standard component exists

System Integration, Scaling and Synchronization

Single chassis for simple systems, but more complex systems need to scale.



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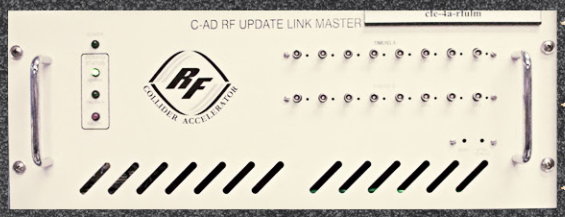
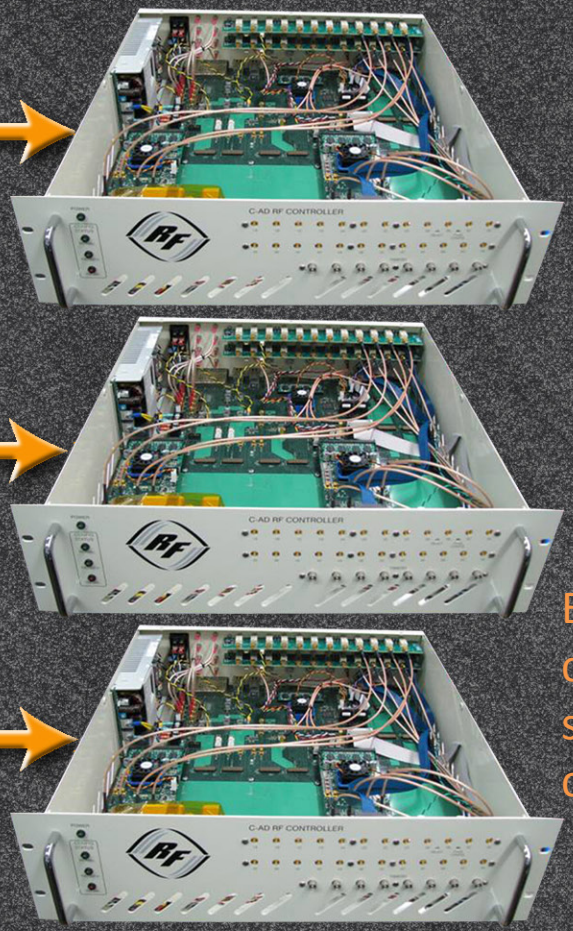
System Integration, Scaling and Synchronization

Single chassis for simple systems, but more complex systems need to scale.

MOP282 - "A Deterministic, Gigabit Serial Timing, Synchronization and Data Link for the RHIC LLRF"



Update Link fiber optic connections



Synchronous capture and broadcast of data

Eliminates constraints on system physical configuration

The Update Link is how we achieve system integration and synchronization.

- Encoded gigabit serial link for:
  - Deterministic timing (coded events)
  - Low latency communication (coded data)

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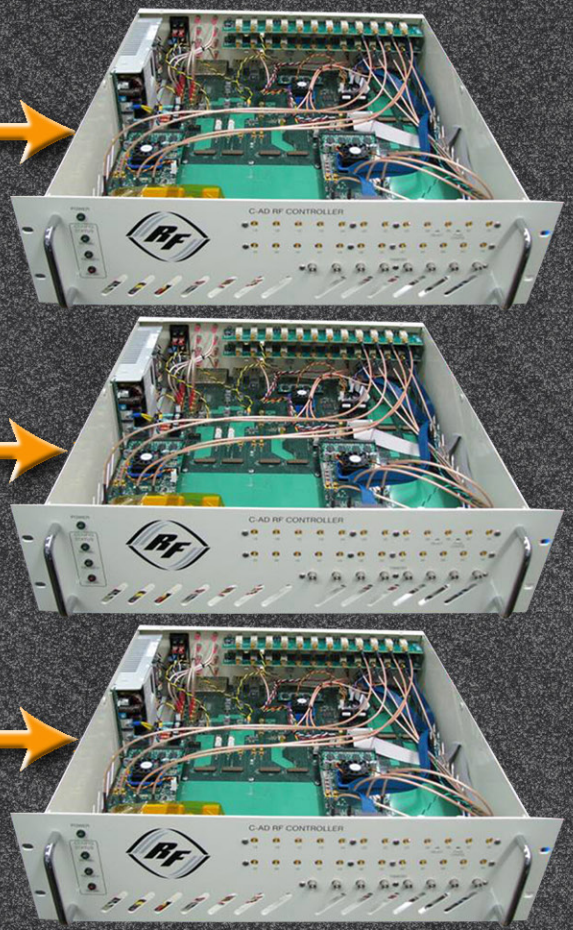
Multi-System "Soft" Reset (Phase Alignment)

Consider 3 RF synthesizers.
Goal: On a trigger, System "B" and System "C" realign phase using System "A" as a reference.

Update Link Master



System "C"

System "B"

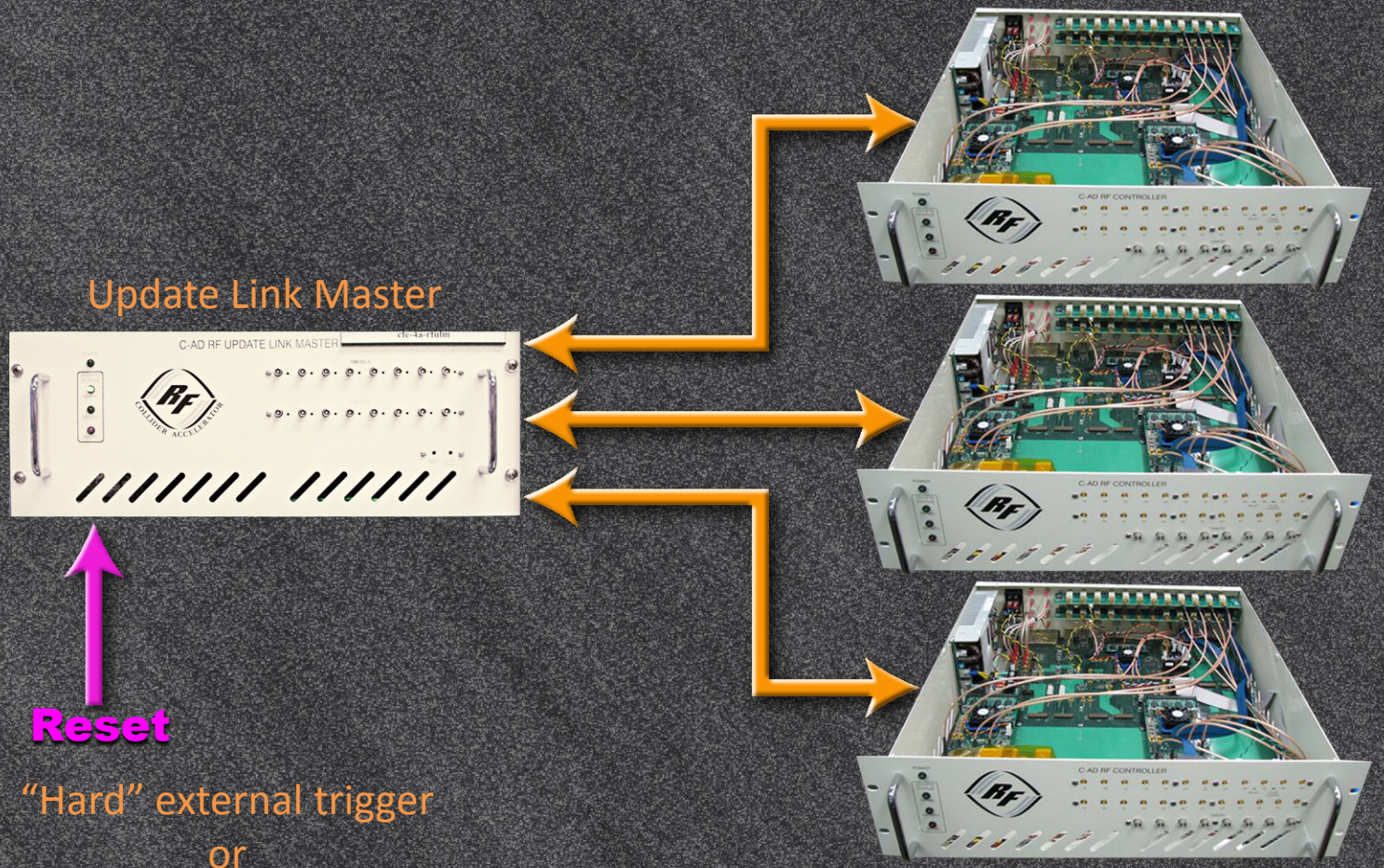
System "A"

Constraints:

System "A" must continue operating unperturbed.

System "B" and System "C" must align to System "A" smoothly. No phase discontinuity.

Multi-System "Soft" Reset (Phase Alignment)



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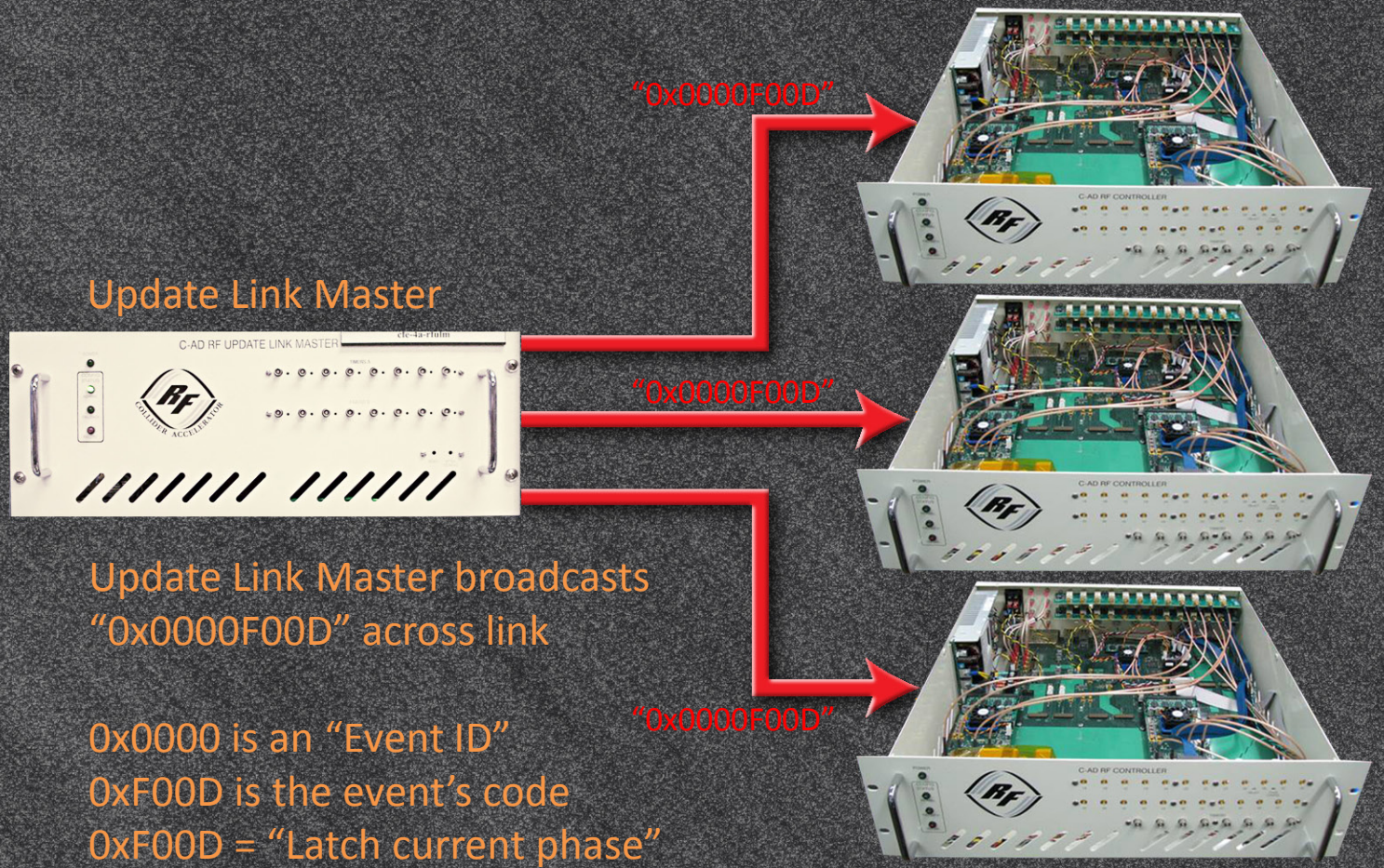
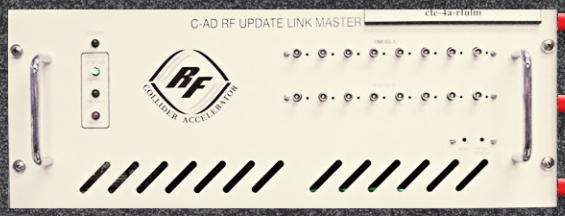


Update Link Master broadcasts "0x0000F00D" across link

0x0000 is an "Event ID"
0xF00D is the event's code
0xF00D = "Latch current phase"

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master



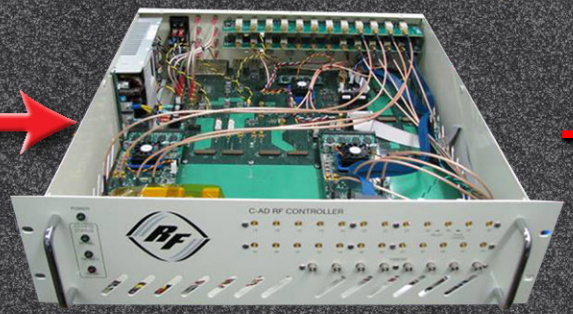
Systems decode "0x0000F00D" as a "Latch Current Phase" event.

90°

System "C"

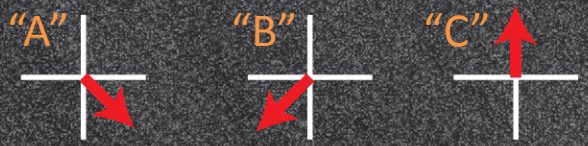
-135°

System "B"



-45°

System "A"



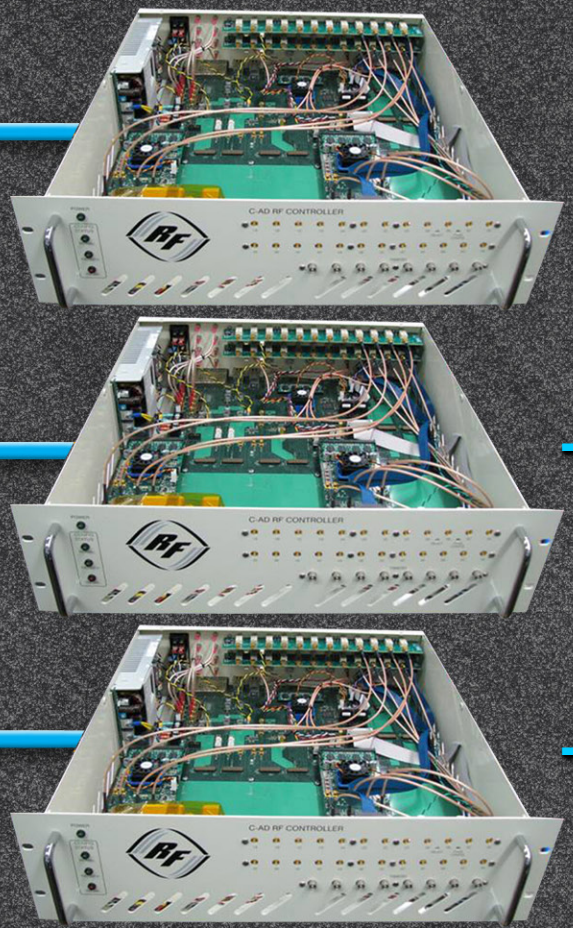
Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

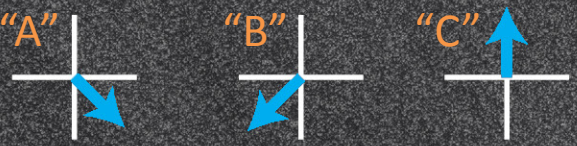
System "A" transmits its latched phase to the ULM, encoded as "0xBEEF0045"

0xBEEF = a data payload ID
0xBEEF = "I am System A's latched phase"
0x0045 = "45°"

"0xBEEF0045"



90°
System "C"
-135°
System "B"
-45°
System "A"



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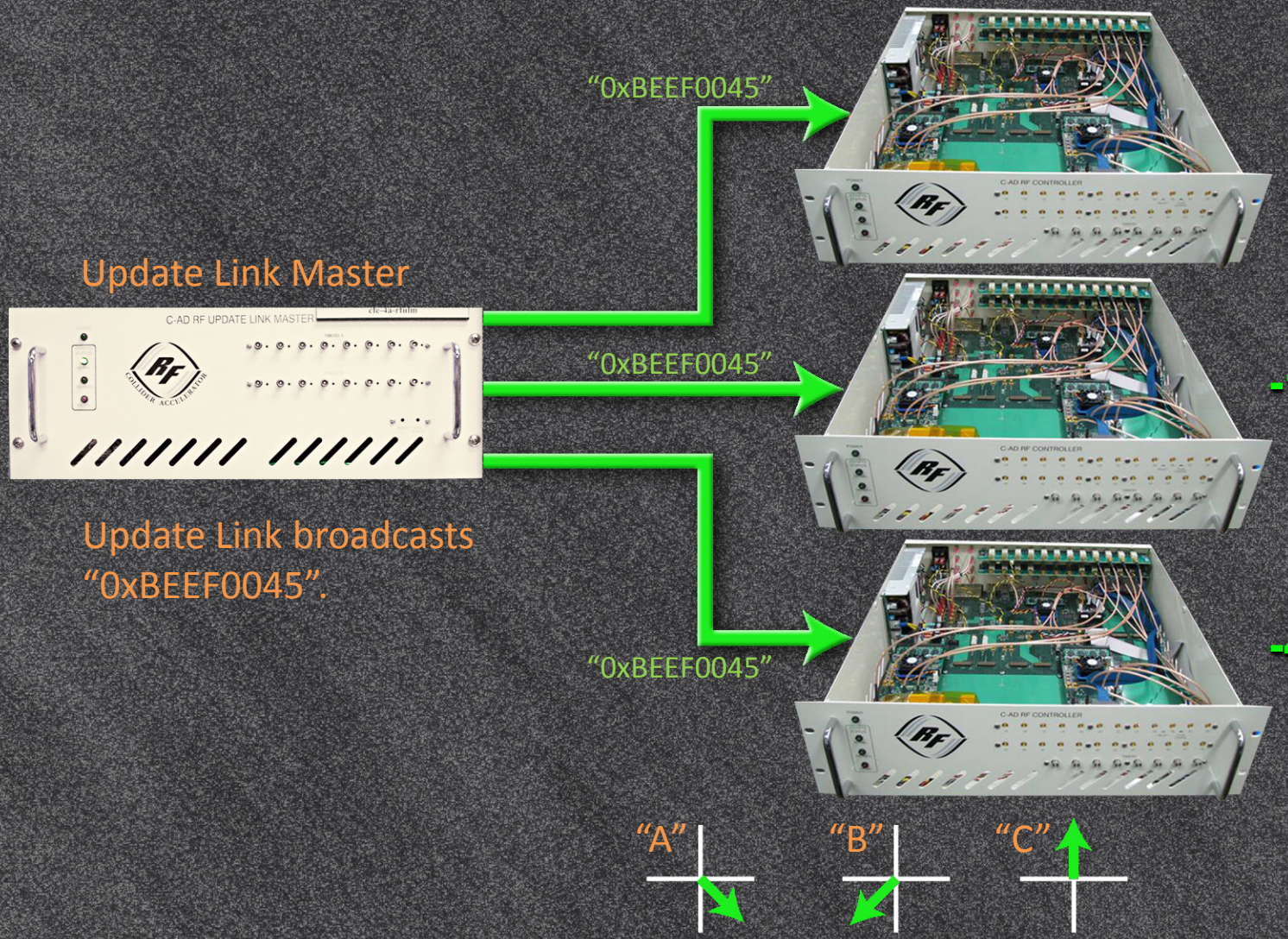

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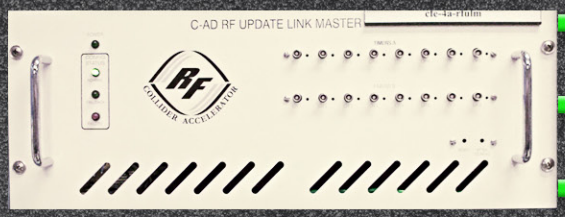
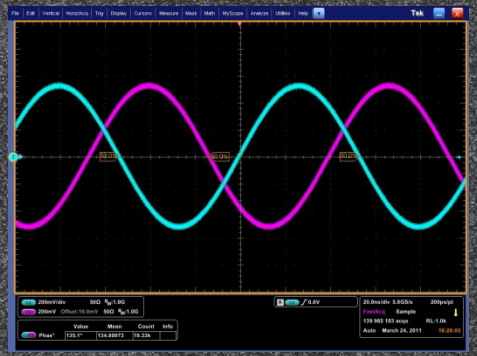
Multi-System "Soft" Reset (Phase Alignment)

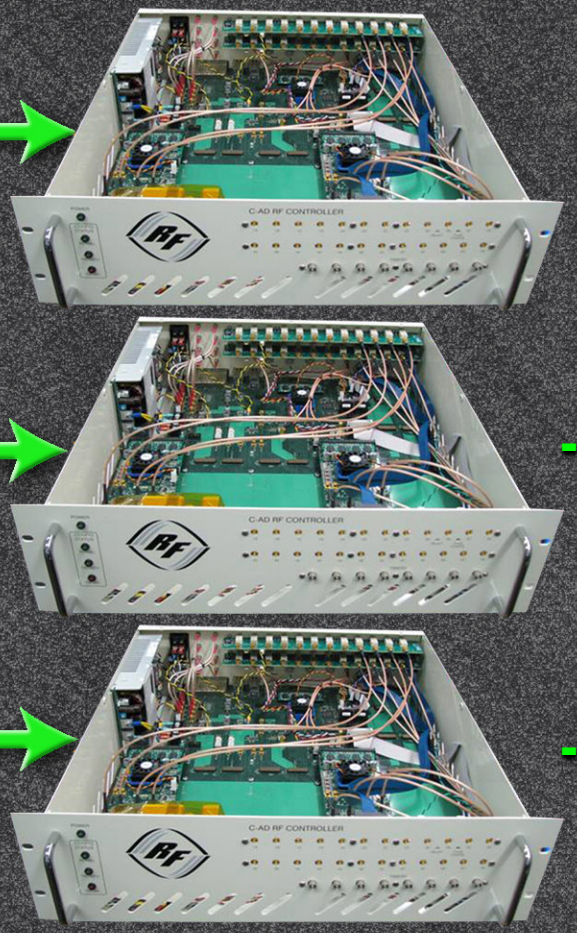
Update Link Master



Systems decode target phase and smoothly cog to target.

System "A" System "C"





90°

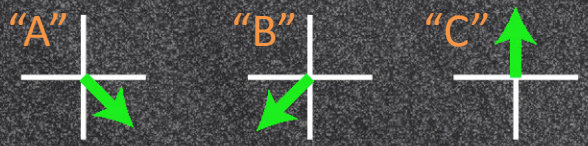
System "C"

-135°

System "B"

-45°

System "A"



Cog by 90°
= -45° + 135°

Cog by -135°
= -45° - 90°

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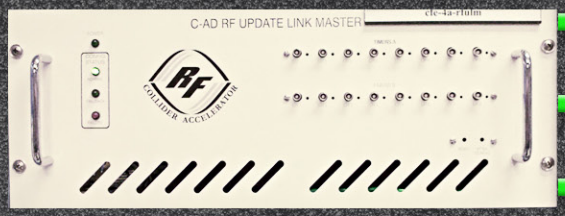
Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

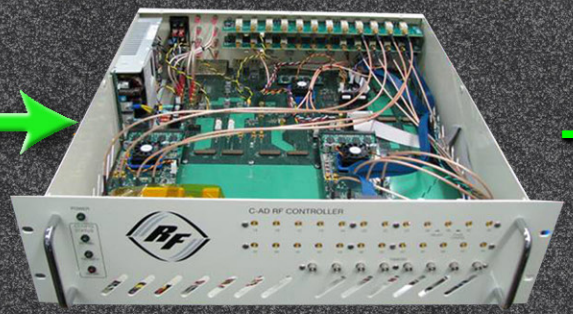


80°

System "C"

-129°

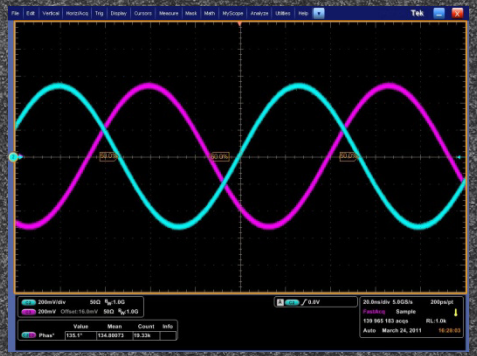
System "B"

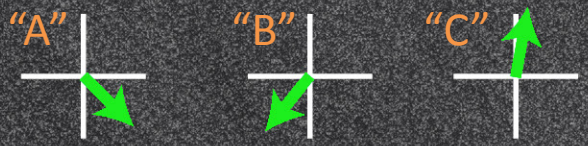


-45°

System "A"

System "A" System "C"





Cog by 90°
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Cog by -135°
= -45° - 90°

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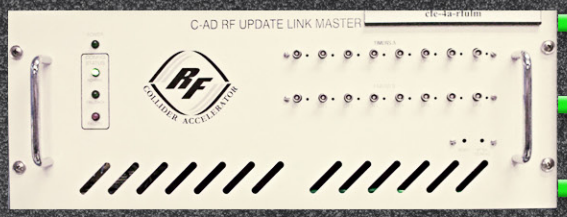
Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

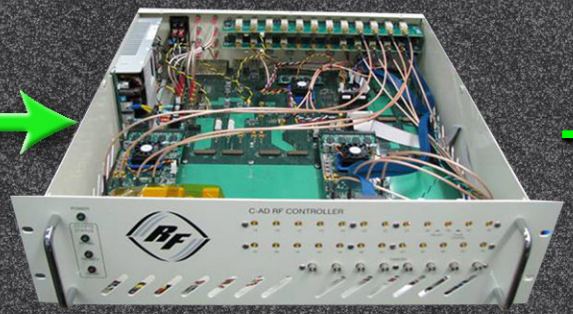


71°

System "C"

-122°

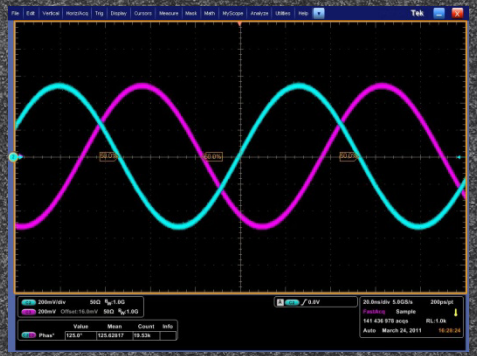
System "B"



-45°

System "A"

System "A" System "C"



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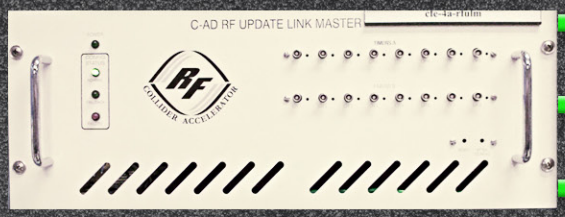
RF ACCELERATOR DIVISION

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

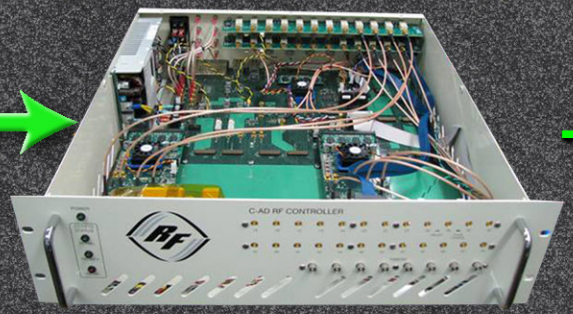


61°

System "C"

-116°

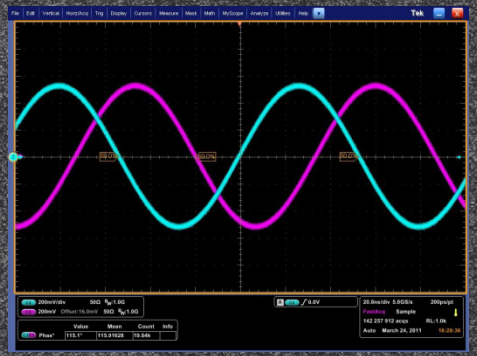
System "B"



-45°

System "A"

System "A" System "C"



Cog by 90°
= -45° + 135°

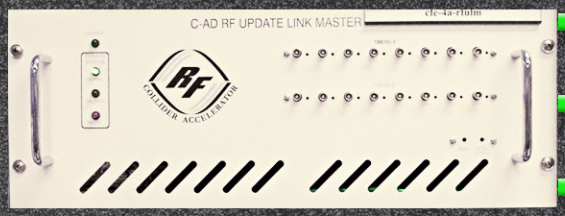
Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

RF ACCELERATOR DIVISION

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

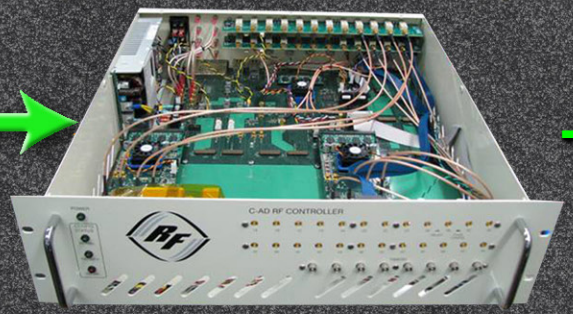


51°

System "C"

-109°

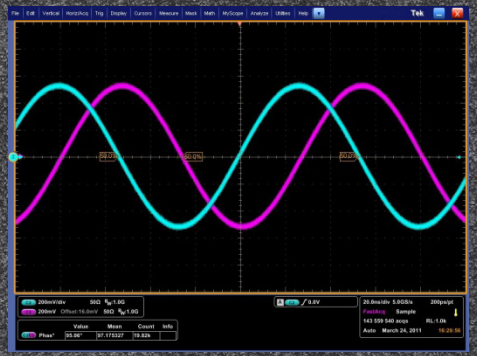
System "B"



-45°

System "A"

System "A" System "C"



Cog by 90°
= -45° + 135°

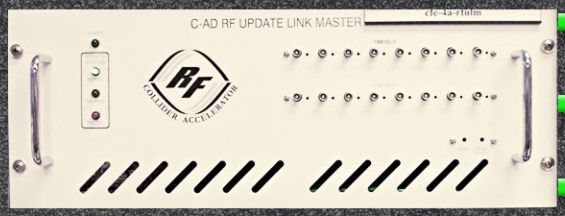
Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

RF ACCELERATOR DIVISION

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master



42°

System "C"

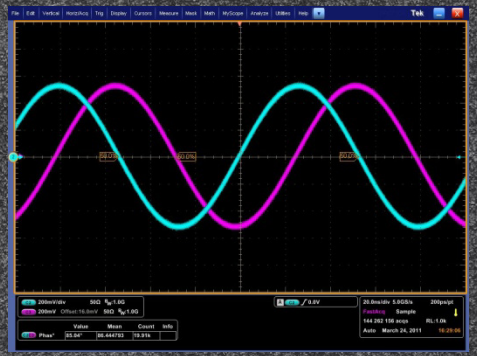
-103°

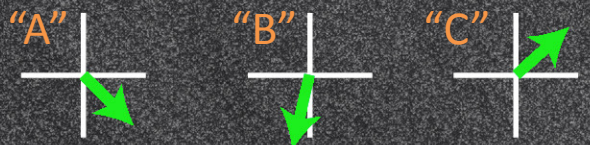
System "B"

-45°

System "A"

System "A" System "C"





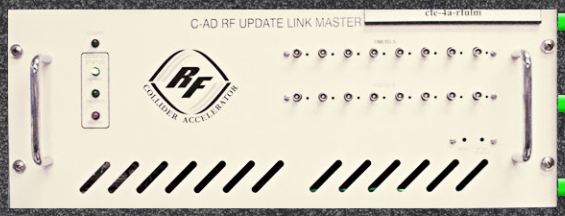
Cog by 90°
= -45° + 135°

Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

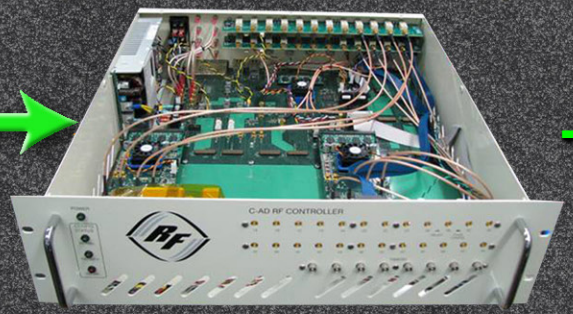


32°

System "C"

-97°

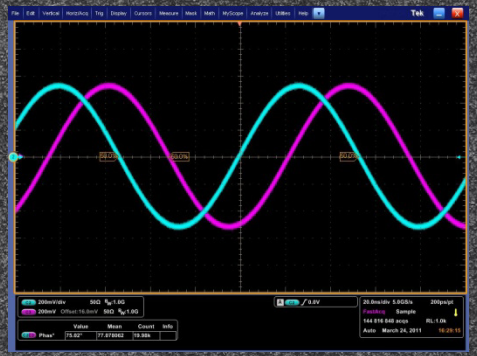
System "B"

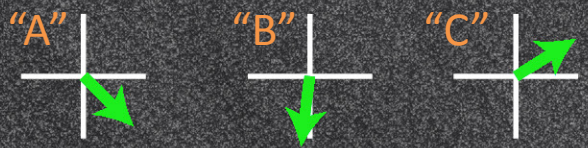


-45°

System "A"

System "A" System "C"





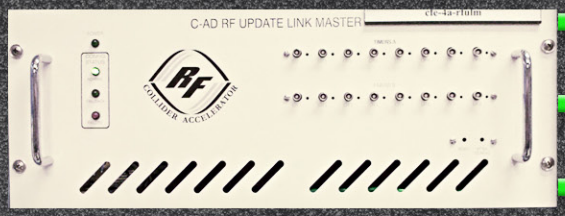
Cog by 90°
= -45° + 135°

Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

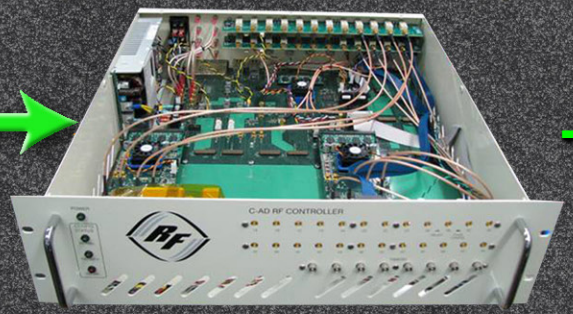


22°

System "C"

-90°

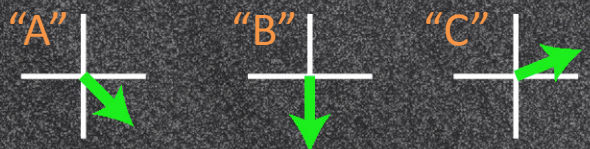
System "B"



-45°

System "A"

System "A" System "C"



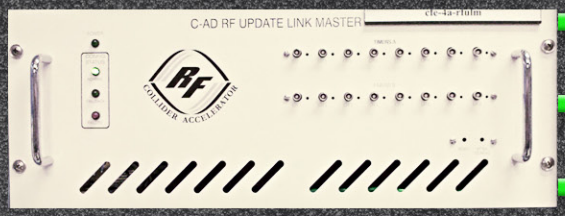
Cog by 90°
= -45° + 135°

Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

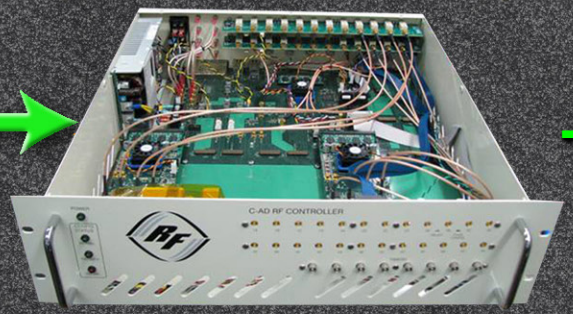


12°

System "C"

-84°

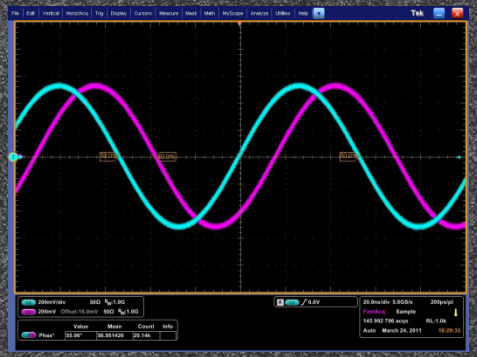
System "B"



-45°

System "A"

System "A" System "C"



Cog by 90°
= -45° + 135°

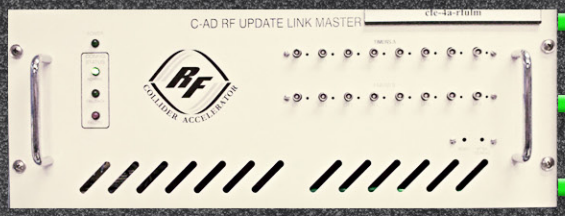
Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

RF ACCELERATOR DIVISION

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

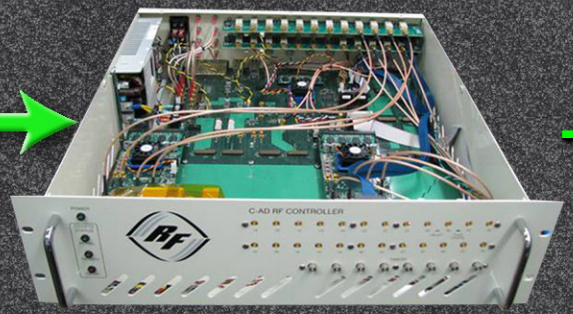


3°

System "C"

-77°

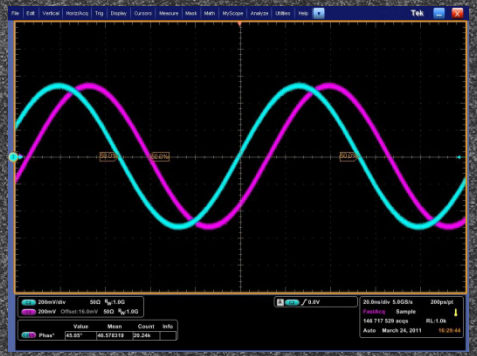
System "B"



-45°

System "A"

System "A" System "C"



Cog by 90°
= -45° + 135°

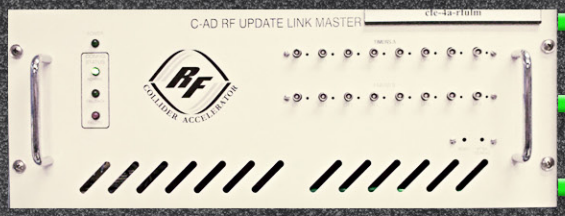
Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

RF ACCELERATOR DIVISION

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master



-7°

System "C"

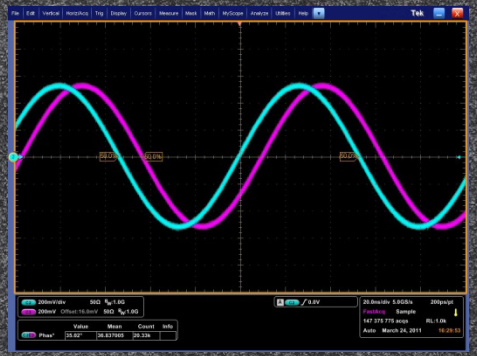
-71°

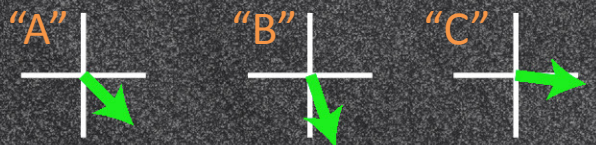
System "B"

-45°

System "A"

System "A" System "C"





Cog by 90°
= -45° + 135°

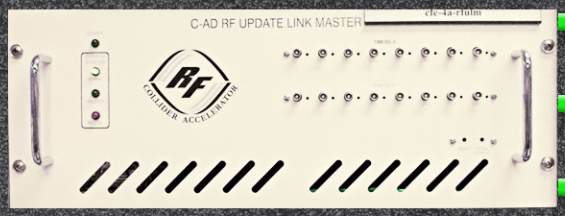
Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

RF ACCELERATOR DIVISION

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

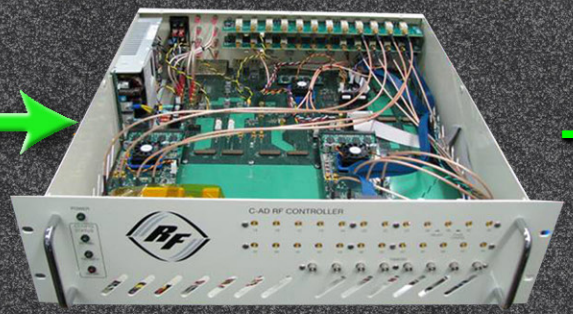


-17°

System "C"

-65°

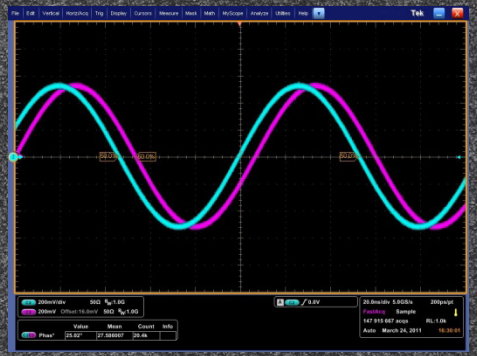
System "B"



-45°

System "A"

System "A" System "C"



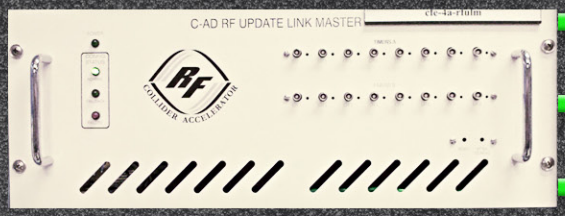
Cog by 90°
= -45° + 135°

Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

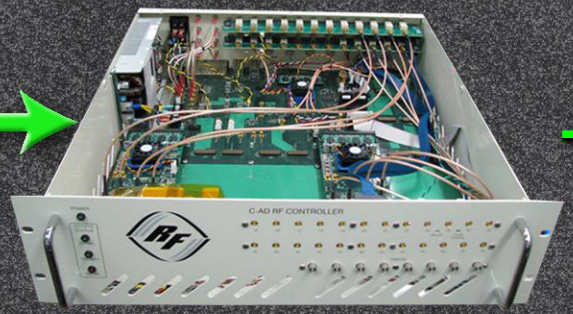


-27°

System "C"

-58°

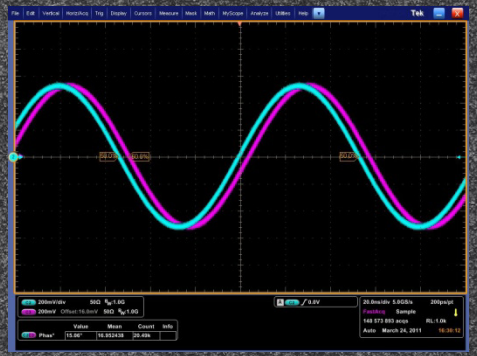
System "B"

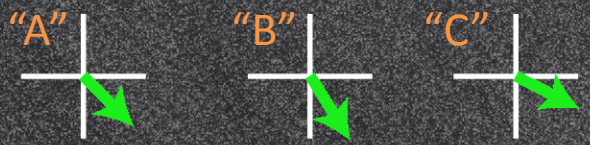


-45°

System "A"

System "A" System "C"





Cog by 90°
= -45° + 135°

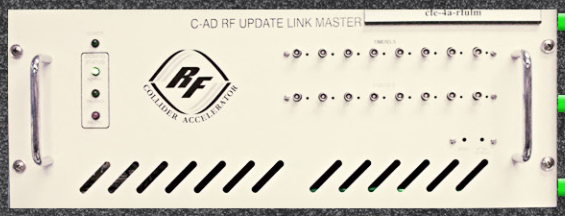
Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

RF ACCELERATOR DIVISION

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

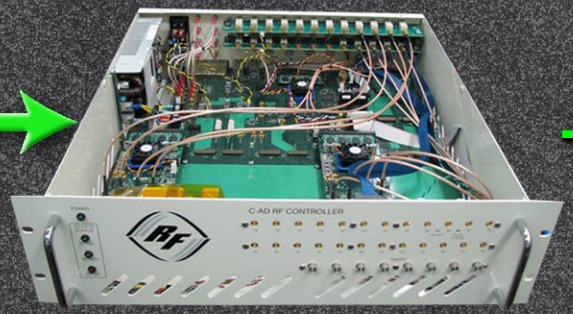


-36°

System "C"

-52°

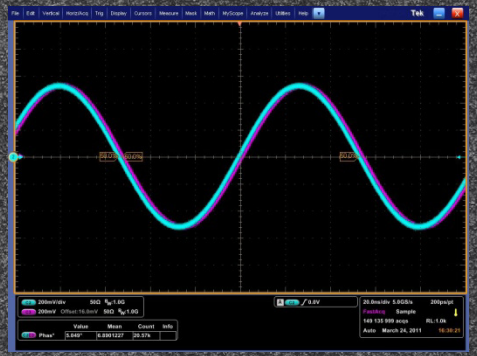
System "B"



-45°

System "A"

System "A" System "C"



Cog by 90°
= -45° + 135°

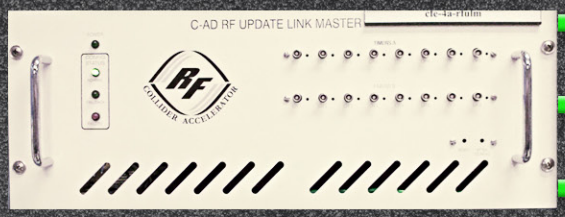
Cog by -135°
= -45° - 90°

BROOKHAVEN NATIONAL LABORATORY

RF ACCELERATOR DIVISION

Multi-System "Soft" Reset (Phase Alignment)

Update Link Master

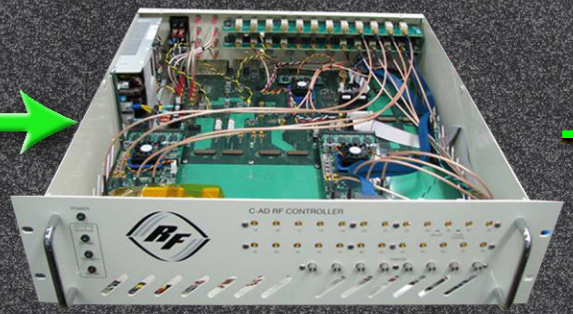


-45°

System "C"

-45°

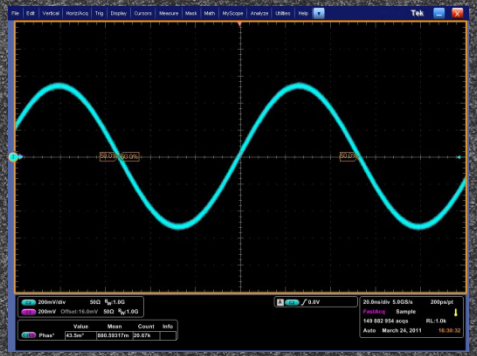
System "B"

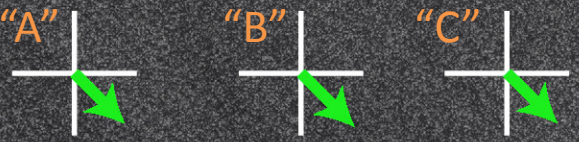


-45°

System "A"

System "A" System "C"





BROOKHAVEN NATIONAL LABORATORY

ACKNOWLEDGEMENTS

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Geetha Narayan
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