COMMISSIONING THE ALS DIGITAL POWER SUPPLY CONTROLLER IN THE BOOSTER DIPOLE AND QUADRUPOLE MAGNET POWER SUPPLIES*

J. Weber#, T. Scarvie, C. Steier, C. Timossi, LBL, Berkeley, CA 94720, U.S.A.

Abstract

The Advanced Light Source (ALS) is a third generation synchrotron light source that has been operating since 1993 at Berkeley Lab. A few years ago, the ALS was upgraded to achieve Top-Off Mode, which required replacing the booster dipole and quadrupole magnet power supplies to increase the peak booster beam energy from 1.5GeV to 1.9GeV. The original analog controller for each power supply has been replaced by a digital power supply controller (DPSC) to improve stability and resolution and provide a remote interface [1]. The DPSC capabilities include 24-bit 100k-point digital reference waveform download and voltage reference generation, and complete digital current loop implementation. The hardware includes an FPGA with an embedded processor running a full EPICS IOC on VxWorks. This paper will present the current functionality of the DPSC as well as performance results from recent commissioning.

INTRODUCTION

The Advanced Light Source (ALS) currently operates for users in Top-Off Mode, in which electrons are injected into the Storage Ring (SR) on energy at 1.9GeV approximately every 15-30 seconds [2]. The Booster Ring (BR) Bend and quadrupole focusing (QF) and defocusing (QD) magnet power supplies were replaced to provide the peak current and accurate tracking required to achieve Top-Off operation.

Figure 1 illustrates a typical injection cycle for the BR Bend, QF and QD power supplies as measured by a precision voltmeter at each DCCT. The x-axis is milliseconds (full scale = 1.4s) and the y-axis is bits on the DVM input. Since each DCCT has a different scaling factor, the amplitudes are not on the same scale. The relative stability and accuracy of these power supplies is critical to achieve stable and reliable injection into the storage ring.

History

The original BR Bend power supply was gated on and free ran up to injection energy uncontrolled, then gated off. The BR Bend field was measured, multiplied by a manually set scaling factor, and added to a 16-bit DAC reference waveform to the BR QF and QD power supplies to track the Bend with adequate accuracy for reliable injection.

The new BR Bend, QF and QD power supplies were each delivered from the manufacturer with a bin of modular electronics that provided control and monitor for the supply. This bin included a digital controller that receives a reference waveform via Ethernet, digitizes the DCCT with a 24-bit ADC, performs the current loop digitally, and generates the voltage loop reference via 20-bit DAC. The voltage loop, Boolean controls, and interlocks were each handled in separate modules. However, unexpected spikes in the digital controller waveforms tripped the power supplies frequently so they were not reliable enough to deliver user beam.

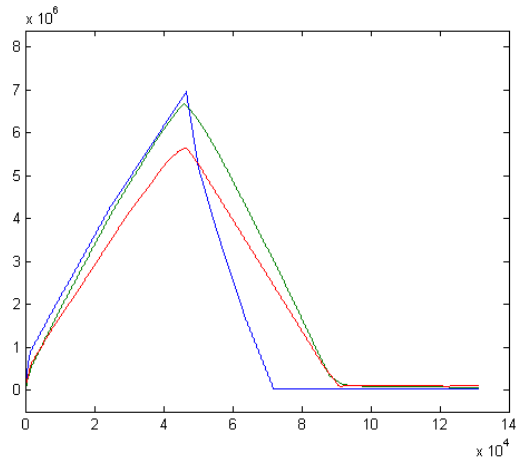

Figure 1: Booster Dipole and Quadrupole Magnet Power Supply Ramping Profiles.

The manufacturer then provided analog controllers that required an external analog reference and lacked a remote interface. The BR QF and QD were re-connected to the original analog reference configuration described above. A Mini IOC [3] DAC output provided the main reference waveform for all three power supplies. Since the analog controller is sensitive to temperature, the BR QF and QD required tuning several times per day to maintain injection efficiency sufficient to operate at continuous top-off energy. The temperature regulation circuit and housing was installed in the analog controller to address temperature sensitivity, reducing the necessity to tune to about once per day.

A new digital power supply controller (DPSC) was designed in-house to improve stability and resolution and provide a remote interface [1]. When the first phase of the DPSC was completed, the controller still required an external analog reference, but the reference and DCCT were digitized, the current loop was performed digitally, and the correction was sent to a 24-bit DAC to provide the voltage loop reference. This phase was done to confirm that the choice of components, including analog

* Supported by the U.S. Department of Energy under Contract No. DE-AC02-05CH11231
#jmweber@lbl.gov

front end, filtering, and data converters, were adequate to meet the performance requirements and that the module was compatible with the electronics bin. Since the same analog reference was used, the BR QD and QF still required tuning about once per day.

Next, the DPSC firmware was modified to add an Ethernet interface allowing remote control and monitoring and download of the digital reference waveform, which is its current form. Since the reference is no longer analog, the stability has improved dramatically such that tuning is only required once per week during machine start-up. This version of the DPSC has been commissioned in all three power supplies as of end of 2010. Figure 2 shows the DPSC installed in the BR QD.

Figure 2: DPSC Installation at Booster QD Power Supply (far left).

SYSTEM DESCRIPTION

In the current implementation, a digital reference table of 2^{17} (~130k) 24-bit values is downloaded to the DPSC FPGA and the DCCT is sampled by a 24-bit ADC. The current loop takes these values as input and generates a correction value sent to the 24-bit DAC. The values are sampled and updated at 100ksps. The DCCT and correction waveforms are stored locally and can be read back for diagnostics. More information about the firmware and software implementation can be found here [1].

The FPGA embedded PowerPC processor runs the IOC software. This complete system-on-a-chip solution runs EPICS on VxWorks providing direct connectivity to the ALS control system. This interface provides remote access for all control and monitor of the power supplies, including waveform readback. Figure 3 shows a DCCT waveform read from the BR Bend DPSC.

Each DPSC receives a *Waveform Trigger* from the ALS timing system initiating each supply's ramp sequence synchronously. When the ramp cycle is complete, the DPSC sends a *Ready* signal back to the timing system to indicate it is ready to receive the next *Waveform Trigger*. There is also a *Simulate* signal indicating that the timing system should automatically switch to *Simulate* mode, which generates injection triggers without ramping the BR Bend for troubleshooting and diagnostics, but this feature has not yet been implemented. The remote on, off, and reset Boolean controls have also been disabled since the remote Boolean interlock and status monitors have not yet been verified.

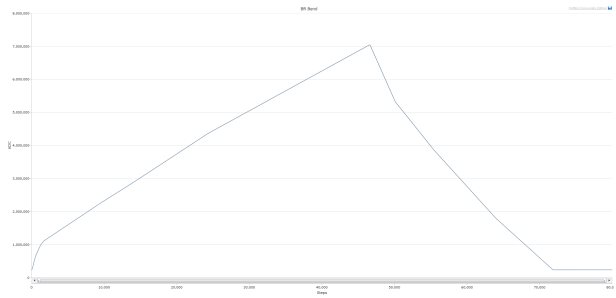

Figure 3: DPSC Digital Waveform of BR Bend DCCT Signal.

OPERATIONAL EXPERIENCE

Since the DPSCs were commissioned with the remote interface, the stability of the Booster has greatly improved over previous configurations. Figure 4 compares injection efficiency before (above) and after (below) DPSC commissioning. The red data is charge entering the Booster and blue data is charge exiting the Booster. According to this data, for similar amounts of injected charge, the efficiency has increased by about 25% and the number of low charge injections (<0.5nC) has significantly decreased.

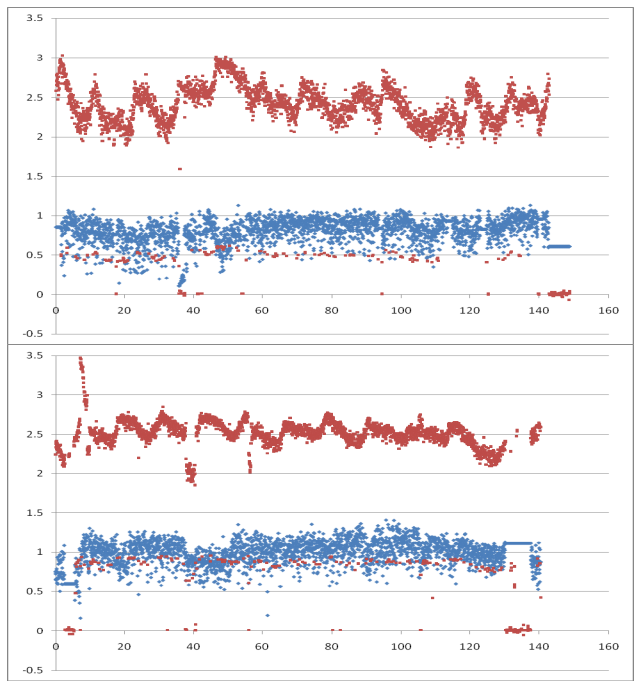

Figure 4: Booster injection efficiency over a one week period of similar operation last year (above) versus this year (below).

However, there are some outstanding issues, in particular with the BR QD, which can prevent reliable tuning.

The main issue is that occasionally an error occurs when attempting to download the full reference waveform to the BR QD. When this happens, sometimes it is not possible to set up and tune the Booster using the normal operating software for extended periods. This problem is intermittent and difficult to reproduce, so the source of the problem has yet to be determined. So far this has been a nuisance at machine start-up, causing delays and a workaround to be developed, but has not resulted in any loss of scheduled user beam time.

The second issue is that downloading a waveform takes many seconds, eliminating the possibility of shot-by-shot tuning (every 1.4s) and causing delays in the tuning process. The download time also varies by many seconds from about 5-20s, and the source of the variation is not well understood.

The last issue is that booting the DPSC takes a very long time—over 10 minutes. At boot time, the DPSC downloads its VxWorks kernel and EPICS software and database configuration over the network. Since the embedded processor only runs at 50MHz, the boot process is slow, but benchmarks indicate it should be faster than it is. We have had a few cases where a DPSC lost its network connection and could only be recovered by rebooting. In these cases the boot time delays restoring control to the unit.

FUTURE CONSIDERATIONS

One potential solution to all the issues is a change in architecture: moving the IOC function from the FPGA embedded processor to a soft IOC and communicating between them with low level networking protocol. Since the embedded processor has fewer resources and much slower processor clock, the soft IOC would boot VxWorks and EPICS much faster, reducing the boot time. This division of labor could also reduce the networking load on the embedded processor and improve download times and reliability. The investigation of this architecture is already underway.

In addition, a feature that allows smaller downloads for tuning is under development as well. This method assumes a base waveform and interpolates a partial new waveform based on a much smaller subset of waveform values. This feature could also significantly reduce the network load during tuning, but will not eliminate the need to download a full waveform after booting.

The hardware also supports additional functionality that has been planned for phased development in the future. First, performing the voltage loop digitally in the DPSC could be done by modifying the electronics bin to connect the voltage measurement into the DPSC ADC originally used as to sample the analog reference, and the firmware to perform the loop algorithm. Then, the IGBTs can be driven directly from the FPGA by mapping the signals to the DPSC module and converting the DAC output value to an IGBT gating waveform. Both phases will require additional research to confirm that the hardware components satisfy the supply performance requirements.

CONCLUSION

The DPSC hardware and firmware performing the current loop, including the data converters and ramping logic, provide accurate, stable, and efficient injection from the booster. Since the ramp control is very repeatable and the relative tracking between power supplies is very good, the long-term reliability has also improved significantly. Adding the remote interface has enhanced control and added additional diagnostics useful for optimizing the reference waveforms.

However, there are some outstanding issues with the remote interface that have prevented reliable access for controlling and tuning the supplies. These issues are currently being pursued, but are elusive to reproduce and therefore difficult to resolve. One option under consideration is a change in the remote interface architecture to shift some of the processing burden to a more capable soft IOC.

Plans for future development include performing the voltage loop calculation digitally and driving the IGBTs directly, although these features require additional bench testing and modifications to the control bin.

Overall, ALS operations have been improved by installing DPSCs in the BR power supplies. The remote interface still requires some effort to improve reliability and make the system more robust, which will complete the first phase of development and commissioning.

REFERENCES

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