RF SOLID STATE DRIVER FOR ARGONNE LIGHT SOURCE

B. Popovic, Argonne National Laboratory & University of Iowa. Iowa City, IA, USA
G. Waldschmidt, Argonne National Laboratory. Argonne, IL, U.S.A

Abstract

Currently, RF power to the APS storage ring and Booster cavities is provided from klystrons with a eventual goal to move to a solid state RF system. A modular design centered around a 1 kW amplifier has been decided on. The driver amplifier was created for this module system using Agilent's ADS circuit simulation software and then built and tested.

INTRODUCTION

Currently, power to the APS storage ring and Booster cavities is provided from 1.1 MW continuous wave (CW) klystrons. Two klystrons provide RF power to the 16 storage ring cavities and a third supplies power to the Booster cavities. Vendors are becoming increasingly difficult to find for replacement klystrons, as a result they are difficult and expensive to replace. The eventual goal is to replace the klystrons and to use a CW 200 kW solid state RF system that consists of 1 KW modules to provide RF to each of the 16 cavities instead.

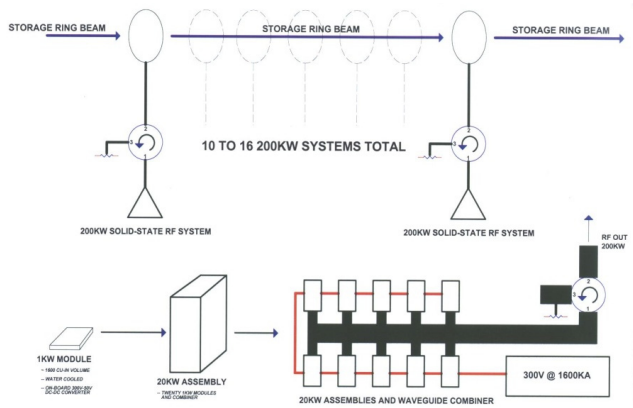

Figure 1: Proposed Solid State Amplifier System using 1kW Modules.

A similar setup is in use at SOLEIL synchrotron outside of Paris, France though the modules are combined to produce 200kW are 330 W each instead of 1kW. APS has chosen to use the Freescale MRF6VP41KHR6 device which produces 1kW CW per module at 352 MHz. The reason for 1kW modules is the available floor space in the RF building, Bldg. 420 at Argonne Laboratory. A larger output power density(W/m^2) is required as a result of the space requirements.

1KW AMPLIFIER MODULE DESIGN

Typically amplifiers consist of multiple stages; in this case the solid state amplifier system will consist of a pre-driver, driver and a final push pull amplifier producing 1kW peak power. Since noise is amplified as well as the desired signal. Low-noise transistors are needed in early stages of amplification

The pre-driver consists of a general purpose amplifier based around Freescale's MMG3014NT1 producing about 20 dBm power output at 1 dB compression. While the driver, the focus of this project and paper, is Freescale's MRF6V2010N, an N-Channel enhancement MOSFET which will output the 10W. Finally, as stated previously, Freescale's MRF6VP41KHR6 push-pull amplifier provides the 1kW output.

Figure 2: The 1kW Amplifier design.

DRIVER AMPLIFIER DESIGN

The focus of much of the work done over this past summer is the driver amplifier design. The rest of this paper will detail the different stages and procedures of the design.

DC BIAS NETWORK

The transistor requires a DC source to bias it. The value for the gate quiescent voltage (V_{GSQ}) is measured from DC curves or just taken from the datasheet for the transistor. While the voltage supply (V_{DD}) value is also listed on the datasheet for the transistor. Usually the DC bias network is just a voltage divider. APS will use a temperature dependent bias circuit using an LM723 integrated circuit to control the gate bias to prevent variation of the device gain. As the temperature increases, the integrated circuit decreases the gate bias, thus reducing the power output and as a result the temperature of the transistor.

Inductors are used as RF blockers to separate the DC bias network from the RF portion of the circuit. Then decoupling capacitors remove any RF signals that are not blocked by the inductors. Finally Ferrite beads remove any RF noise that may have been included with the DC source.

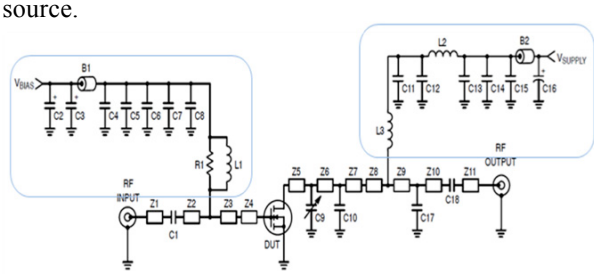

Figure 3: Driver circuit shown with DC networks circled.

In figure 3 the RF blockers are L1, L2 and L3. While the ferrite beads are B1 and B2. The decoupling capacitors are all of the capacitors in the DC network.

CREATING MATCHING NETWORKS

Matching networks are created based on the results from the Load/Source Pull analysis, in the case of the driver amplifier: Z_{source}= 6.2 + j28.8; Z_{load} = 35.4 + j28.3. Lumped element inductors and capacitors are then used for matching elements. In addition to the lumped elements, distributed elements such as the microstrip transmission lines must be incorporated into the matching network. Matching networks may be created visually on the Smith chart, with ADS providing a Smith chart tool. Various topologies may be investigated.

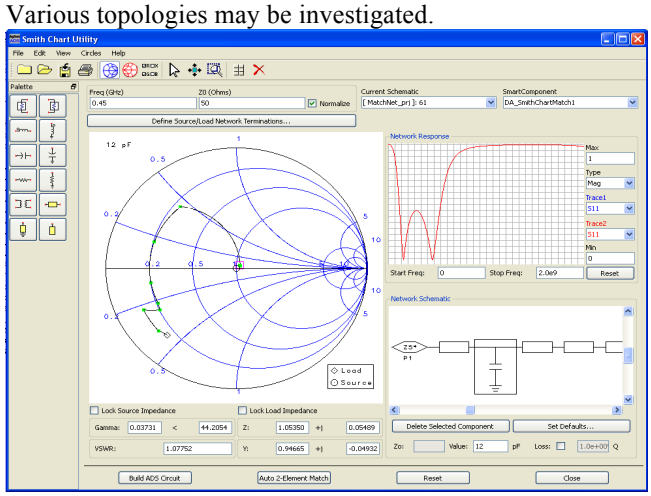

Figure 4: ADS Smith Chart Utility with matching network created.

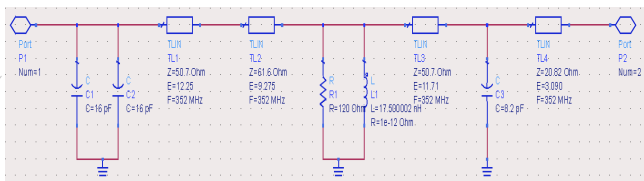

Figure 5: Input Matching Network for 450 MHz MRF6V2010N Driver.

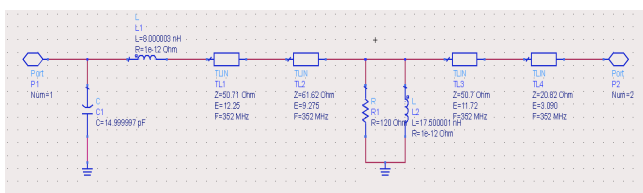

Figure 6: Output Matching Network for 450 MHz MRF6V2010N Driver.

CIRCUIT BOARD PROTOTYPING

A prototype of the driver PCB was etched using the circuit prototype, Quick Circuit 3000, available to the RF group. IsoPro software is used to load the CAD drawings and then modify them to program the prototyper. The files include the placement and sizing of the traces, vias and screw holes.

Figure 7: Quick Circuit 3000 prototyper.

The PCB board itself consists of a substrate sandwiched between to copper layers. The prototyper uses various bits to drill the vias and screw holes. It then etches the traces by removing the copper layer of the board using a specialized bit. Finally it cuts the specific PCB board's shape out of the larger PCB. Then the vias are filled with bailbars in order to connect the top and bottom ground planes electrically.

DRIVER PROTOTYPE

The board was brazed to a copper carrier for thermal conductivity and also to enlarge the ground plane. The lumped elements were then soldered on and then finally the transistor. The transistor is thermally connected to the copper carrier with thermal grease. After successful operation it will be soldered to the carrier for improved thermal contact, along with better DC contact between the transistor source and ground.

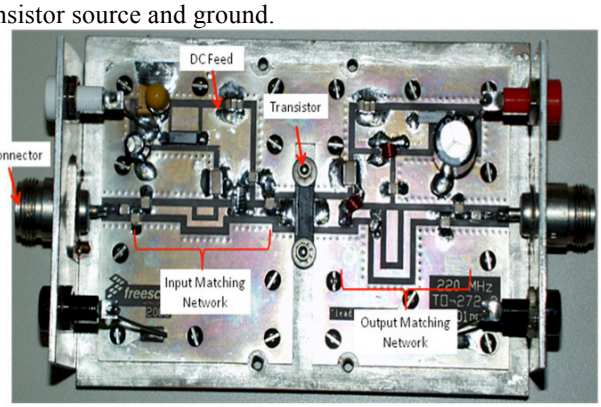

Figure 8: Prototype driver amplifier.

TEST AND MEASUREMENT

A function generator at 352 MHz was used for the RF input. While a 30dB commercial amplifier was used to amplify the signal from the function generator to 20 dBm into the driver amplifier. Separate DC supplies were used for the gate and drain voltages. A power meter was used to measure the output power.

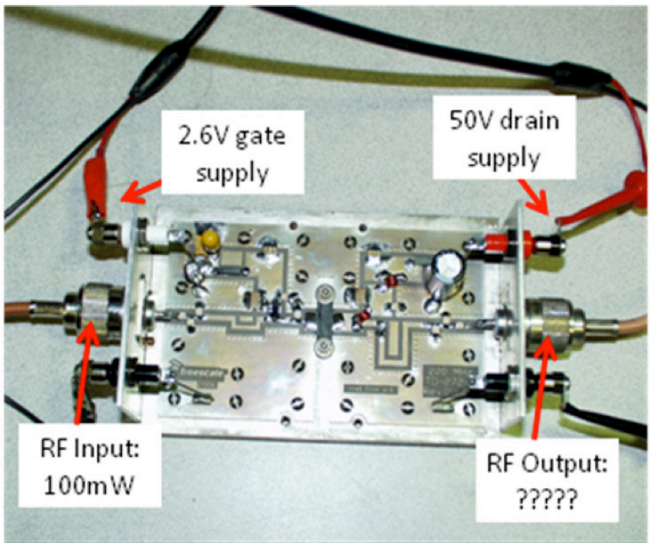

Figure 9: Driver amplifier connected to the test setup.

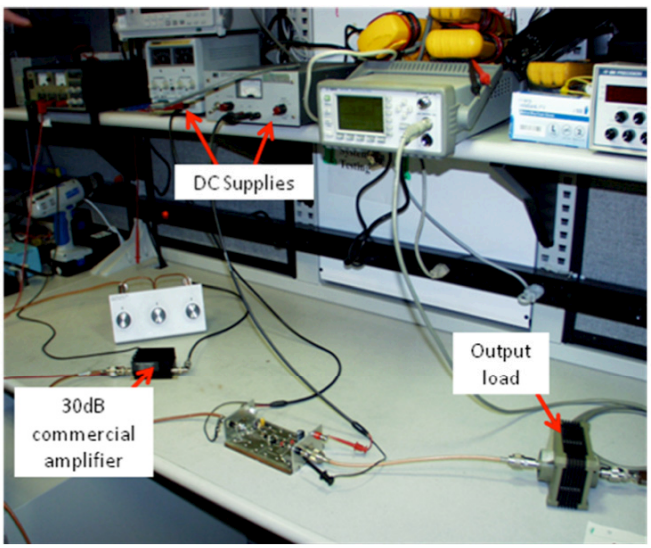

Figure 10: Driver amplifier test setup.

MEASUREMENT RESULTS

The driver amplifier was measured from 100 mW to 10 W output. While the gain was measured to be 19.3 dB compared with the simulated value of 20.1 dB. Finally the driver efficiency was measured to be 48.9% at 10.4W output power with the simulated drain efficiency at 50.1%. These are preliminary results, with more performance possible as a result of fine tuning the input and output networks. The capacitor positions on the microstrip can be adjusted to possibly provide even more gain. Also there are alternate matching networks that have been simulated that could be employed to further optimize the circuit.

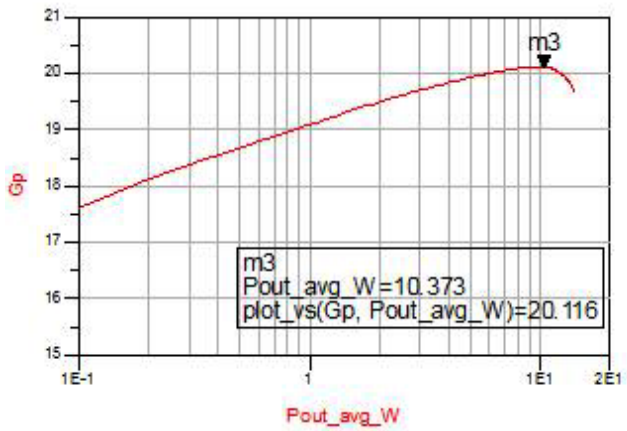

Figure 11: Simulated driver amplifier gain.

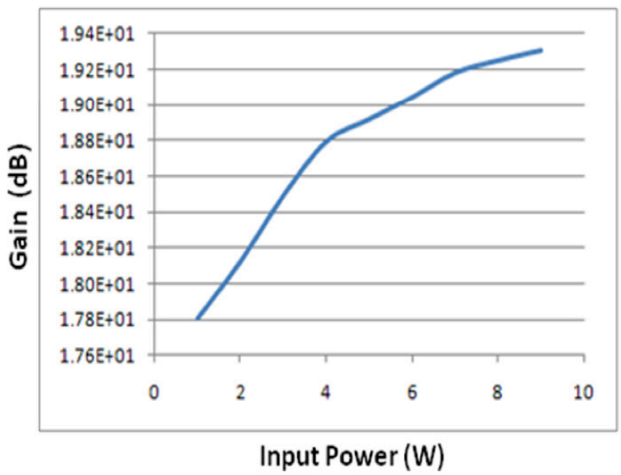

Figure 12: Measured gain of driver amplifier.

ACKNOWLEDGEMENTS

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