Knife-Edge Thin Film Field Emission Cathodes*

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Abstract

Cathodes made of thin-film field emission arrays (FEA) have the advantages of high current density, pulsed emission, and low bias voltage operation. We have developed a technology to fabricate knife-edge field emission cathodes on (110) silicon wafers. The emitter geometry is optimized for efficient modulation at high frequency. Cathode fabrication progress and preliminary analysis of their applications in RF power sources are presented.

I. INTRODUCTION

The RF power sources needed for future e^+e^- linear colliders and RF-linac-driven FEL's both require an electron source with the capability of emitting electrons in high density pulses. Traditional dispenser cathodes used in klystrons, for example, provide a d.c. current density $\leq$10 A/cm^2 and require a buncher to achieve pulsed beams. The bunching process usually increases the beam emittance and introduces instability limits to bunch currents and length. As an alternative, our gigatron project [1] features a gated field emitter array that produces pulsed electron beams in the form of ribbons. The ribbon beams are accelerated in a diode, and then pass through a traveling wave coupler where the RF power is extracted. By eliminating the bunching process and minimizing the transit of bunched beam to the output coupler, extreme beam stability and excellent RF efficiency should be feasible to attain. The first demonstration of emission from FEA's was reported by Spindt *et al.* at SRI [2]. Gray [3] and many others [4] have also actively worked to develop FEA's for vacuum microelectronics. Spindt's FEA's have produced current densities as high as 1000 A/cm^2 from an area of $\sim$1 mm^2 [4], but the frequency modulation achieved is below 1 GHz [5]. For the gigatron it is necessary to develop a new type of FEA which can support efficient modulation and high current density at frequencies $\geq$10 GHz. The focus of this work is to fabricate knife-edge thin film field emission cathodes on (110) silicon wafers. Preliminary studies show that this cathode can meet the requirements of the gigatron.

II. FIELD EMISSION ARRAY CATHODES

The Spindt-type FEA is so far the most successful FEA cathode. Its structure is shown in Figure 1(a). The emitter is a metal cone sitting at the center of a cavity formed on a metal-insulator-semiconductor sandwich structure. The top metal layer serves as the modulating gate. When a voltage is applied between the gate and the substrate, a electric field E concentrates near the tip of the cone and can support field emission. The emitted current density J is described by the Fowler-Nordheim equation [6]:

$$J = AE^2\exp(-B\phi^{3/2}/E)$$

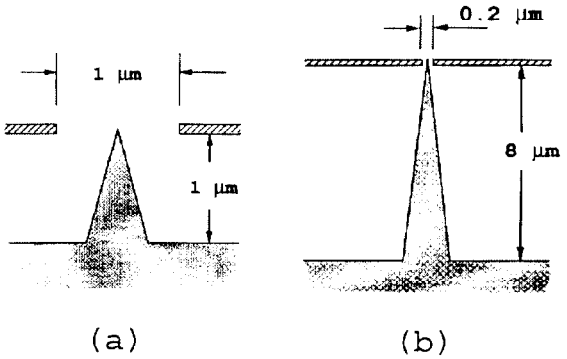

Figure 1. The cross section geometry of Spindt-type FEA (a) and the knife-edge FEA (b).

where A and B are two parameters close to constant and ϕ is the work function of the emitter material. For high performance FEA's, it is desired to have large current emission at low bias voltage. This requires that the emitter structure is designed to maximize the field at the emitter apex. This includes a small emitter radius and a small gate opening. The Spindt-type FEA has a tip radius around 500 Å, a gate diameter of about 1 μm, and a gate/base gap of about 1 μm. With these dimensions, the emission starts with $\sim$100 V bias. For modulated emissions, however, the Spindt-type FEA's have a drawback: the gap between the gate and the substrate is small and the sandwich structure presents a large parasitic capacitance to the modulation driver. The cutoff frequency is $f_T = g_m/2\pi C$, where g_m is transconductance of the emitter, $g_m = (\Delta I_c/\Delta V_g)|_{V_c}$. Spindt has improved the fabrication process to reduce the overlapping area between the gate and the base layers, but this only increases the estimated f_T to $\sim$1 GHz.

The gigatron is designed to operate at 18 GHz or higher frequencies; for this goal, we have proposed a new fabrication approach [7] that makes knife-edge field emission arrays (KEFEA) on (110) silicon wafers. A cross section of the structure is shown in figure 1(b). We have increased the gate/base gap to about 8 μm and reduced the gate opening to $\sim$0.2 μm. The capacitance per unit area is reduced thereby by a factor 20 from Spindt-type FEA's. Figure 2 shows a POISSON [8] simulation of the

* Work supported by U.S. Department of Energy, Office of High Energy Physics, under contract no. DE-FG02-91ER40613

0-7803-1203-1/93$03.00 © 1993 IEEE

potential distribution in both the Spindt-type FEA and our KEFEA structure. The smaller gate opening in the KEFEA produces higher field for the same voltage bias, with lower parasitic capacitance. Both effects increase the transconductance.

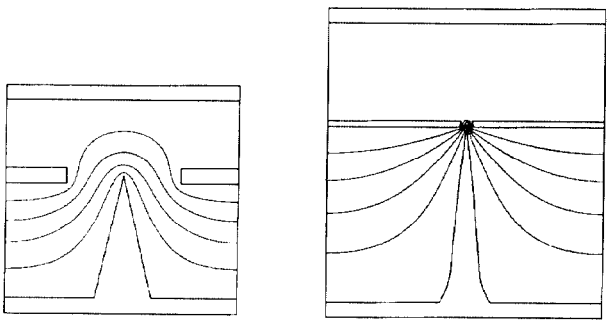

Figure 2. POISSON simulations showing the equipotential lines of Spindt-type FEA (a) and KEFEA (b).

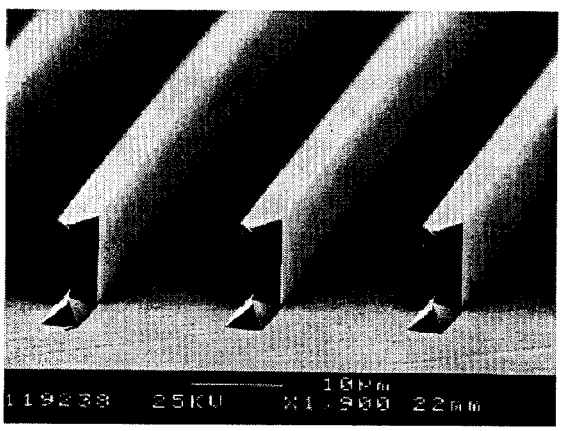

Figure 3. SEM picture showing the wall structure formed by KOH solution etching.

III. FABRICATED STRUCTURE OF KEFEA

The fabrication starts with a plain (110) silicon wafer. We use photolithography to put down a SiO_2 pattern of width $\sim$4 μm. Orientation-dependent etching of the wafer in a KOH solution forms a structure as shown in Figure 3. The silicon is etched along crystal planes to produce rectangular prisms $\sim$10 μm high, which serve as the "blanks" from which the knife-edges will be formed. A second etch in a solution made of HF, HNO_3 and CH_3COOH (Dash etching) sharpens the top portion of the wall-like structure (Figure 4). The cross section of this knife-edge is very similar to that of Figure 1(b), with an edge half angle of about 5°. Our measurement from a scanning electron micrograph (SEM) shows that the radii of these etched edges are less than 500 Å. To further reduce the knife-edge radius, we use a thermal oxidation process to grow a surface layer of SiO_2 into the knife-edge structure. The oxidation process is carried out at temperatures below 1000°C, and serves to sharpen the corner at the top of the Si/SiO_2 interface. Our measurement shows that the edge radius obtained this way is less than 200 Å. A study by Marcus *et al.* [9] has shown that a radius of 10 Å can be obtained in this way.

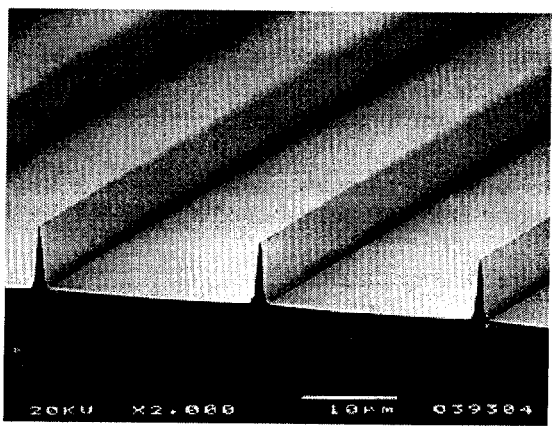

Figure 4. The knife-edge array formed on a (110) silicon wafer.

The insulator material used in the Spindt-type FEA is SiO_2, which has a dielectric constant of 3.9. For the KEFEA, we use a layer of polyimide coating (PI). PI has a lower dielectric constat (2.9 to 3.3), giving a further reduction of capacitance. We apply the polyimide as a spin-on liquid with a layer thickness of $\sim$10 μm. This allows us to make the knife-edge structure $\sim$8 μm high. When PI is applied, it planarizes above the knife edges. The PI is then etched in an O_2/CF_4 plasma which isotropically removes $\sim$3 μm of the PI material, and exposes the top $\sim$1 μm of the knife edges. The top edges of the native silicon inside the SiO_2 layer is then located at about at the same level as this etched PI surface.

The metal used for the gate layer is applied using RF sputtering, with a thickness of $\sim$0.5 μm. We then apply a layer of photoresist and etch it back to expose the top portion of the metal covered knife-edges. The metal layer is then etched to expose the SiO_2 layer over the knife edge. Using a HF solution we then strip away the SiO_2 to expose silicon emitter edge. Since we can precisely control the thickness of the thermally grown SiO_2 layer, we can produce a gate-emitter spacing $\sim$0.1 μm.

Figure 5 shows the finished structure of our KEFEA. The height of the emitter and the gate/base gap is about 8 μm. The emitter-edge is at the same level as the gate. The metal is etched back and a gap is opened over the knife edge. (This sample was overetched, giving a wider gap than that of our design.)

IV. DISCUSSION

The challenges for modulating FEA cathodes at microwave frequency are:

- shrinking the control gap to enhance transconductance and reduce transit time;
- isolating the gate from the substrate to reduce parasitic capacitance.

In KEFEA we have devised a means to fabricate knife-edges with extremely small edge radius and gate/edge gap. The thermal oxide process is key to achieving both features. It sharpens the tip radius to $\sim 100\mathring{A}$, and provides an accurate means of making a controlled gap of ~ 0.1 μm between tip and gate. This process is a new development in vacuum microelectronics and produces the same field enhancement factor at a knife-edge as the best enhancement attained on Spindt-type tips.

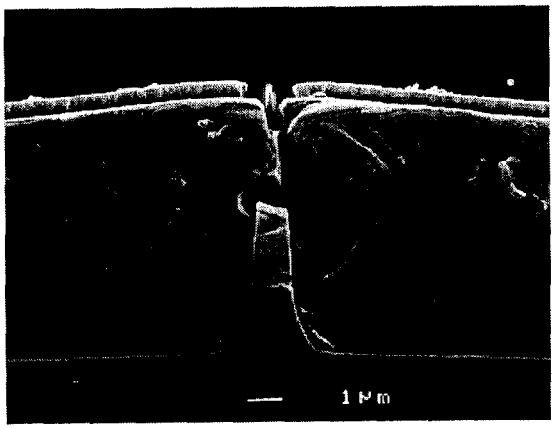

Figure 5. SEM picture of KEFEA structure.

Using orientation-dependent etching to prepare the knife-edge blanks and spin-on polyimide to build the dielectric support for the gate layer, the gate-base separation can be increased and the parasitic capacitence reduced by a factor of 10 compared to Spindt-type tip arrays.

Field emission from any emitter geometry always occurs at a microscopic region (hot spot) where the work function is lowest or the surface features most irregular. Emission from adjacent regions is suppressed by space-charge even as electric field is increased. Studies of field emission from tip arrays have shown that only a single ~nm-sized hot spot emits on each tip. The maximum practical emitter density (3 μm tip array) is $\sim 10^7/\mathrm{cm}^2$.

By contrast the KEFEA geometry should produce emission from hot spots which are spaced along the edge by a separation comparable to the edge/gate spacing (the spacing at which adjacent regions are isolated from one another's space charge). For a 10 μm knife-edge spacing and an edge/gate gap of 0.1 μm, the emitter density should be $\sim 10^8/\mathrm{cm}^2$.

The improvements – high field concentration, 10 times less parasitic capacitance, and 10 times more in emitter density – translate directly into improved transconductance and bandwidth. The ultimate high-frequency limit would come from transit time in the edge/gate gap. For a modulation ~10V and a gap of ~ 0.1 μm, the transit time would be $\sim 10^{-13}$ sec, corresponding to a cut-off frequency $f_T \sim 400$ GHz.

Present development of the KEFEA technology has achieved all of the process steps. Currently the edge/gate geometry is being fine-tuned in the final etch steps, and initial emission experiments will begin soon. One direction for further development is the possibility of depositing a low-work-function material onto the finished tip surface. Candidate materials include CVD diamond and cermet. The development of modular KEFEA cathodes for the gigatron and other applications is in progress.

V. REFERENCES

[1] P.M.McIntyre, H.M.Bizek, S.M.Elliott, A.Nassiri, M.B.Popovic, D.Raparia, C.A.Swenson and H.F.Gray, "Gigatron", *IEEE Trans. Electron Dev.* **ED-36**, No.11, 2720 (1989).

[2] C.Spindt, I.Brodie, L.Humphrey and E.Westerberg, "Physical properties of thin-film field emission cathodes with molybdenum cones", *J. Appl. Phys.* **47**, No.12, 5248 (1976).

[3] H.Gray, G.Campisi and R.Greene, "A vacuum field effect transistor using silicon field emitter arrays", *IEDM Tech. Dig.*, 776 (1986).

[4] Special issue on Vacuum Microelectronics Conference, July 1990, *IEEE Trans. Electron Dev.* **ED-38**, No.10 (1991); Proceedings of the Fifth International Vacuum Microelectronics Conference, *J. Vac. Sci. & Tech. B* **11**, No.2 (1993).

[5] C.Spindt, C.Holland, A.Rosengreen and I.Brodie, "Field-emitter-array development for high-frequency operation", *J. Vac. Sci. & Tech. B* **11**, No.2, 468 (1993).

[6] R.H. Fowler and L.W. Nordheim, "Electron emission in intense electric fields", Proc. Roy. Soc. London, ser. A 119, 173 (1928).

[7] B.Lee, E.Barasch, T.Mazumdar, P.McIntyre, Y.Pang and H.-J.Trost, "Development of knife-edge field emission cathodes on (110) silicon wafers", *Appl. Surface Sci.* 67, 66, (1993)

[8] Los Alamos Accelerator Code Group, The POISSON/SUPERFISH Group of Codes, LA-UR-87-115 (January 1987), version 4.12 (17 March 1993).

[9] R.Marcus *et al.*, "Formation of silicon tips with <1 nm radius", *Appl. Phys. Lett.* **56**, No.3, 236 (1990)