© 1993 IEEE. Personal use of this material is permitted. However, permission to reprint/republish this material for advertising or promotional purposes or for creating new collective works for resale or redistribution to servers or lists, or to reuse any copyrighted component of this work in other works must be obtained from the IEEE.

RF Synchronous Transfer Into Specific Buckets Between Fermilab Main Ring And Tevatron Accelerators

K. Meisner

Fermi National Accelerator Laboratory*

Abstract

I present a description of the design philosophy, hardware implementation, and operation of the system used to place beams transferred in either direction between the Main Ring and Tevatron accelerators into specified RF buckets of the receiving machine. The system provides reliable phase coordinate placement with .09° resolution without beam measurements of any kind. The system also controls the collision point in the Tevatron during the Fermilab colliding beams HEP program with .689 mm. resolution.

Introduction

During early preparations for the first Fermilab colliding beams operation, it was realized that a new method of RF synchronous beam transfer was required between the Main Ring (MR) and Tevatron (Tev) accelerators. Special functionality for these transfers includes accurate phase coordinate placement into specific RF buckets, minimal disturbance of beam previously injected, transparent bidirectional transfer operation, accommodating very low intensity beams of protons or antiprotons, the ability to completely test the system without beam, and remote control and diagnostic capability. In early 1984 a hardware system to accomplish these goals progressed from design to installation. It has since provided reliable operation and has become known as the Cogging LLRF system.

Principle of Operation

RF synchronous transfer is the correct beam to RF bucket phase at injection. Synchronization between any two Fermilab accelerators means both accelerator RF cavity systems have equal frequencies and a specific, adustable phase relationship between them at beam transfer time. Fermilab LLRF systems traditionally use phase lock loops to synchronize one machine to another. Since the final conditions are achieved from arbitrary frequency offset and phase initial conditions, the phase lock loop approach can present problems when RF buckets contain beam. Fast RF bucket phase modulation from transient effects and loop initial conditions should be avoided. Beam momentum deviations also should be minimized.

The cogging system provides synchronization while avoiding these problems. The basic principle of the cogging system is to drive the RF cavities of both the MR and Tev accelerators from the same LLRF oscillator at transfer. The Tev LLRF oscillator is a synthesizer with an output frequency that is very stable and accurately programmed from a bend magnet current input, and is chosen to be the common RF drive source.¹ Accurate control of the relative phase between the drive signals to the RF cavities of each machine then correctly places beam into the RF buckets in the phase coordinate. An output of the Tev LLRF oscillator that does not drive any RF cavity is frequency modulated to exactly match the MR LLRF output frequency and phase, and is then switched in to drive the MR RF cavities, with no observable effects on the MR beam. The modulation is generated digitally, and is relaxed in a very controlled manner.

After synchronization to an arbitrary RF bucket is complete, a process called transfer cogging aligns the beam to a specific bucket by again frequency modulating the Tev LLRF signal and MR RF cavities. This modulation produces any required integral bucket shift between MR and Tev. MR and Tev beam synch clock system (MRBS and TVBS) markers label the RF buckets of each machine.² These clock systems generate markers at the beam revolution frequency by continuously dividing RF outputs from the respective LLRF systems by the harmonic number. The MRBS marker is also used to synchronize MR beam injection to a specific RF bucket. Transfer cogging components of the cogging system measure and adjust MRBS and TVBS marker (bucket) displacement, and so do not require actual beam measurements for operation or system tests.

Frequency modulation of the Tev LLRF signal is accomplished by the MR Cogging Delta Frequency (MRCDF) module. This is one application of many DF module uses at Fermilab. DF modules are digitally controlled, bi-directional, fully periodic RF phase shifters. They can receive a 12 bit phase shift input program to produce $\Delta\Phi$, and they can receive a clock pulse train (Fclk) and sign control input to produce $d/dt (\Delta\Phi) = +/-\Delta F$. The Tev LLRF system also uses two DF modules, one each to control the drive signal phase shift to the Tev proton and anti-proton RF cavities. These are called Proton Cogging DF (PCDF) and Anti-Proton Cogging DF (APCDF) modules.

Figure 1 shows elements of the cogging system, the MRBS and TVBS systems, and the MR and Tev LLRF and RF cavities. Nine control sequences accomplish RF synchronization and transfer cogging. A tenth sequence adjusts the proton-antiproton collision point in the Tev, and is called collision point cogging. A module named the Cogging DF Controller (CDFC) accepts accelerator timing information and coordinates all cogging operation.

Cogging DF Controller

The CDFC module decodes TCLK to determine current MR cycle cogging requirements. Cogging control sequences begin and end when specific events are detected by the CDFC, and generally require arbitrary amounts of time for completion. The CDFC provides precise control of the MRCDF module and specifies the MRCDF phase with a resolution of Φ Lsb = 360°/4096 = .089°. The CDFC also controls the MRCDF d Φ /dt = Δ F and d² Φ /dt² = Δ Fdot with resolutions of .125 Hz and .250 Hz/msec respectively.

The CDFC contains an accurate voltage to frequency converter (VFC) that can be driven by several input voltages,

^{*} Operated by Universities Research Association Inc., under contract with the U.S. Department of Energy.

and selects which input runs the VFC with FET switches. Any selected input drives a comparator to obtain the sign of Vin. An absolute value circuit converts Vin to -1Vinl x gain in order to drive the VFC. Each VFC output pulse steps the MRCDF phase 1 Lsb when enabled by the CDFC.

The CDFC contains a 12 bit DAC that can also drive the VFC. A 12 bit counter (Δ Fcounter) loads the DAC, and provides knowledge of the MRCDF module Δ F magnitude. The Δ Fcounter can itself be clocked at a controlled rate, and therefore specify the MRCDF Δ Fdot. This clock rate is determined in the CDFC by an 8 bit \pm N circuit driven by a stable 500 Khz TTL oscillator.

The CDFC contains a 12 bit arithmetice logic unit (ALU) with selectable A and B inputs used for detecting control sequence start and end events (A=B), A versus B magnitude comparisons, and subtractions required in CDFC calculations. The CDFC also contains a 22 bit phase "tick" counter that sums MRCDF phase increments (VFC pulses) and counts MRCDF revolutions to an accuracy of 1 part in Mrevolutions*4096.

Cogging Control Sequences

This section describes the ten cogging control sequences.

Sequence 1 occurs at Tclk event C1 once each Tevatron load cycle before any beam is injected. The CDFC clock decoder detects event C1 and presets Tev LLRF PCDF and APCDF modules to phases specified by host computer parameters T:PCDFP and T:APCDFP. This sequence resets fractional RF bucket collision point cogging from previous Tev cycles and specifies the Tev RF cavity phases for subsequent beam transfers.

In sequence 2, the MR LLRF system accelerates the beam to flattop. As the MR 150 Gev flattop begins, the MR LLRF system VCO and beam feedback loops are controlling the beam. The MRCDF module is off (Δ F=O), and it's output frequency equals the Tev LLRF oscillator programmed value. A Fermilab overlap phase detector (OPDET5) compares the MR LLRF signal to the Tev LLRF output of the MRCDF module and shows a beat frequency between the two signals. The Tev LLRF output can successfully drive the MR cavities only if it is very near the 150 Gev programmed frequency. Hardware called the Permit module reads the Tev energy program, compares it to the 150 Gev value, and inhibits or allows a trigger named M:LMRCDF (Lock MRCDF).

Sequence 3 and those which follow occur only if the LMRCDF trigger is passed to the CDFC by the Permit module. CDFC FET switches select OPDET5 Vout as the VFC analog input (Vt) to close a high gain phase lock feedback loop (PLL). This forces the MRCDF RF output into a constant phase relationship with the phase shifted MR VCO RF, and modulates the TLLRF frequency in whatever direction is required to equal the MRRF frequency. The CDFC Δ Fcounter and DAC are also preset to zero in this sequence.

Sequence 4 begins after the PLL has remained closed for 18 msec. The CDFC DAC is then ramped up from zero at a fixed rate of 62.5 Hz/msec. A sample of Vt is low pass filtered and compared to the DAC output (Vd). When a CDFC analog comparator detects Vd=Vt, the Δ Fcounter stops to hold Vd, OPDET5 Vout is disconnected from the VFC (Vt

decays to zero volts) and Vd is switched into the VFC. The CDFC latches and remembers the sign of ΔF , and applies this information to the MRCDF +/- ΔF control input. At this time the CDFC also pulses the select B input of two MRLLRF system RF switches so that the MRCDF output drives the MRRF cavities, the MR beam, and the LLRF distribution system (the MRBS input source). The MRCDF output frequency and phase is identical to the VCO RF, but is derived from the Tevatron LLRF oscillator, and is precisely controlled by the ΔF counter, DAC, and VFC in the CDFC.

Sequence 5 begins the relaxation of the MRCDF frequency modulation. To make algorithms of sequence 6 a function of one independent variable, ΔF is programmed to 50Hz. The CDFC ALU compares ΔF to 50Hz (ΔF nom) and ramps the ΔF counter up or down as required toward 50Hz at a $|\Delta F$ dotl rate of 1.04 Hz/msec. The ALU monitors $\Delta F(t)$ and stops changing the ΔF counter when $|\Delta F|=50$ Hz.

In sequence 6 the CDFC calculates the Δ Fdot rate at which the MRCDF frequency must go from Δ F=50Hz toward Δ F=zero. The rate is derived by comparing the current MRCDF phase reading (Φ r) to the desired stop phase (Φ d). Φ d is an input from the host computer named M:MRCDFP. As the MRCDF approaches Δ F=O, the area of Δ F(t) Δ T must be such that the integrated MRCDF phase steps (slippage) will smoothly approach Φ d=M:MRCDFP from the MRCDF initial phase= Φ r The CDFC ALU finds (Φ d- Φ r), and uses this to address prom tables that load N into the \div N circuit to control the Δ Fdot rate.

In sequence 7 the CDFC ALU compares $|\Delta F(t)|$ with 1 Hz (ΔF lim). When it detects ΔF =1Hz, the CDFC holds ΔF and continues reading $\Phi r(t)$, the MRCDF phase. When $\Phi r = \Phi d = M$:MRCDFP, the CDFC inhibits further VFC tick pulses to the MRCDF and forces ΔF =0. At the completion of sequence 7, the Tevatron and MR RF systems are driven by one oscillator and have exact relative phasing. RF synchronous transfer to an arbitrary RF bucket is possible. For the fixed target physics program (only one beam transfer per Tev cycle) sequence 7 is the final cogging system function. The Tev bucket which receives the first beam bunch is then labeled bucket 1 by a clock lock process in the TVBS system.

Tclk events E20, E2A, and E2B designate Main Ring cycles for the Fermilab colliding beams program. Sequence 8 and 9 provide transfer cogging, and occur on any of these cycles. Single MR bunches are loaded into the Tev on sequential MR acceleration cycles. At the start of sequence 8 the MR bunch azimuthal location with respect to the target Tev RF bucket is arbitrary on each cycle. The target bucket is unique for each cycle and bunches must be injected with roughly equal spacing around the Tev circumference. A bucket offset is applied on each injection cycle to the TVBS marker which labels bucket 1. The Cogging Zero Shifter (CZS) module applies the offset by shifting the the TVBS marker an interval specified by host computer parameters C:XCBO (transfer cog bucket offset). Transfer cogging then always brings the MRBS marker into alignment with the offset TVBS marker. The CDFC issues a pulse called CSBREQ (Cogging Smart Box Request) at the end of sequence 7. The pulse interrupts a micro processor in the Cogging Smart Box (CSB), which begins the following sequences to generate a $\Delta F(t)$ waveform to drive the CDFC VFC and MRCDF module:

1)Trigger the Cogging Phase Detector (CPD) to measure the bucket displacement between the MRBS and offset TVBS markers as PHASE=buckets to cog. Send PHASE as a digital word (CSBBS in figure 1) to the CDFC.

2)Calculate PHASE*GAIN/TIME. GAIN and TIME are CSB parameters input by front panel thumbwheel switches. This calculation determines the maximum amplitude of the $\Delta F(t)$ wave form.

3)Send a REPLY pulse to the CDFC to initiate transfer cogging. The CDFC selects the CSB output wave form as the VFC drive (Vt). The CDFC also presets its tick counter to PHASE and begins to count down with each VFC pulse sent to the MRCDF module.

4)The CSB outputs a word called Cogging Phase Detector Phase Compare (CPDPC) to the CPD and continues reading the RF bucket displacement (PHASE).

5)When PHASE = CPDPC, the CSB ramps the voltage wave form to a "vernier level", which is also a CSB input parameter. The CSB continues reading PHASE from the Cogging Phase Detector.

Sequence 9 begins when the CSB reads PHASE = 1 from the CPD and there is just 1 bucket left to cog. The CSB

then ramps its $\Delta F(t)$ output wave form to a small value that produces $|\Delta F| = 2Hz$. The CDFC tick counter keeps track of how many buckets the beam is actually cogged and will stop the MRCDF at exactly the correct phase (Φd -M:MRCDFP) when the tick counter reaches 0. At this point RF synchronous transfer into the specified Tev bucket is possible.

Sequence 10 controls collision point cogging and occurs on interrupt from the host computer. Parameters T:ACPS and T:MCPS specify integer bucket and fractional bucket cogging shifts respectively. The CDFC selects a Δ F rate of ±2Hz (or 2 buckets per second) and frequency modulates the Tev LLRF APCDF module and shifts the four anti-proton RF cavities and beam azimuthally relative to the protons. A one bucket shift via ACPS cogs the antiprotons a distance of the (orbit circumference ÷ 1113), the harmonic number, and moves the collision point one half that amount. Fractional cogging via MCPS provides 2⁻¹² of a single bucket shift, which equals .689 mm. A parameter named C:COGSUM sums all collision point cogging displacements.



References

 K. Meisner, et al., "A Low Level RF System For The Fermilab Tevatron", IEEE PAC proceedings (1987)
D. Beechy and R. Ducar, "Time And Data Distribution Systems At The Fermilab Accelerator", Nuclear Instruments and Methods in Physics Research A247 (1986)