Controls Interface Protocols for the SSC Correction and 'DC' Magnet Power Supplies

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Abstract

The control, monitoring and diagnostic requirements of power supply systems determine the required functionality (or transactions) and response of the interface protocol. Advances in technology allow increased functionality of front end control equipment and therefore relatively sophisticated interfaces are required. The protocols to be used must be capable of supporting functionality upgrades. The command response type protocols standardized on earlier are no longer adequate. This paper describes the interface protocol to be used between the SSC Corrector and 'DC' magnet power supplies and their respective controllers. Factors affecting protocol definition and constraints placed by cost and availability considerations are described as well as an implementation strategy.

I. INTRODUCTION

Magnet power supply control requirements for the SSC Global Accelerator Control System (GACS) are determined by many factors. The SSC Global Accelerator Control System must support the operation of the 10 hz cycling LINAC and the Low Energy Booster (LEB) on the one hand, while at the same time it must be capable of supporting the 20 hour flat-top operation of the collider. Special requirements are additionally imposed by the large number of devices involved, the large distances spanned and by the demanding availability requirements placed on the collider.

The SSC GACS interfaces to sub-system' controls for major systems such as the RF and Cryo. The interface to the magnet power supply controls is at the sub-system level for the Ring magnet and the Kicker magnet power supply systems, while for the 'DC', the Pulsed and the Corrector magnet systems[1] it is at the equipment interface level.

Figure 1 is a representation of the generic GACS equipment level interface to magnet power supply systems. The

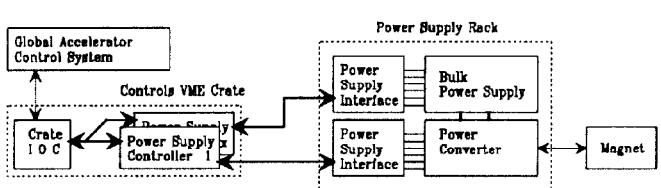

Figure 1: Power Supply Controls Block Diagram

boundary between the GACS and the magnet power supply system is the link between the power supply (equipment) controller and the power supply. The GACS interfaces to processors at the VME crate level called Input Output controllers or IOCs. The IOCs talk to VME crate based power supply controllers which are connected to power supply interfaces by fibre optic links. The power supply interfaces hide power supply particulars such as type (bulk or power converter), reference resolution and output current level, from the controller. Configurations can differ from that shown in figure 1. For example each of the LINAC 'DC' power supplies will be independent. There will be no shared bulk power supply.

In the above controls architecture the interfaces between the GACS, the Crate IOC, the power supply controller and the power supply all need to be defined (the power supply to magnet interconnect is defined elsewhere). The earlier choice of EPICS as the controls software platform for the SSC GACS defines primary interaction of the GACS with the Crate IOC. The physical interface between the IOC and the power supply controller is the VME crate backplane. The data transfer protocols between the IOC and the equipment (in this case power supply) controller level affects GACS characteristics such as process synchronization and are to be defined elsewhere. An instance of this interface is to be described for the LINAC 'DC' power supply controllers in reference [2]. This paper discusses the equipment control protocol between the power supply controller and the power supply for the SSC Corrector, Pulsed and 'DC' Magnet power supplies.

A. *Requirements*

Design goals are to reduce the number of controllers types and to use common protocol format across Machines and power supply types. The control protocols chosen must be capable of supporting as subset the collected requirements of the Corrector, Pulsed and 'DC' power supply controls.

Details of protocol such as command and data formats for the various power supply types depend on the required functionality (control, monitoring and diagnostic) for each of these types and are described elsewhere, for example[3].

The GACS interfaces to the power supplies through three control levels. The protocol must allow the use of power supply interfaces that do not require local intelligence, reducing the software and maintenance support required.

The protocol must support timely delivery of command & data and the synchronization of actions across the site. For the LEB correctors a reference update rate of 10 khz with a delivery accuracy of ± 2 μS is required.

The protocol must allow expansion to include foreseen requirements such as: the use of special methods for meeting the high availability requirements of the SSC accelerator complex[4], or the expected use of these controllers for other applications requiring either set-point controllers or ramp generators synchronized to the machine cycle, eg. the ramp generators required for the Beam Loss Monitor Bias supplies and tune kickers.

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B. Choice of Protocols

Various alternative protocols were explored including the SSC Message Broadcast system (MBS) protocol[5]. Advantages would have been common hardware components and reusable support software. However the ± 5 μS message granularity (as determined the 1.54 Mhz T1 carrier and the MBS frame definition) would not meet the delivery accuracy requirement. The MBS variable length frame left open the possibility of timing inaccuracies exceeding tolerances being inadvertently introduced at a later date.

A command response type protocol is inappropriate since it would require intelligence at the power supply interface for interpreting received commands. A free running protocol, in which status information is continuously returned, was chosen. Requirement for delivery accuracy was met by specifying fixed frame size, with each frame delivering a specific command or reference data and by specifying required link speed. Delivery requirements for other high speed applications may be met by using higher speed links limited by the minimum packet size that can be used.

II. CONTROLS INTERFACE PROTOCOLS

Functionally the interface can be considered as a layered system along the lines of the ISO Open Systems Interconnect model, which consists of the applications, the presentation, the

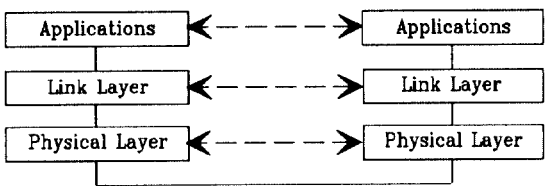

Figure 2: Power Supply Control Protocol Layers

session, the transport, the network, the data link and the physical layer. The power supply controller to power supply link is a point to point link. The presentation, the session, the transport and the network layers can be considered null since corresponding functionality requirement does not exist or is minimal. Figure 2 is a data flow diagram showing the physical data paths and the logical interconnects. The functionality of each of the layers (except the physical interface) may be implemented in either hardware or software. The following sub-sections discuss the functionality and implementation choices for the each of the layers.

A. The Application level protocol

Protocol data flows for the ramped and the set-point controllers are as described below. Correction magnets reference (and optionally command information) is sent from the power supply controller to the power supply interface every 100 μS for the LEB correctors (1 mS for all other machines), during normal operations. Reference and commands received at the power supply interface are loaded into predetermined registers. Receipt of a reference value triggers a series of events overseen by a hardware timing controller at the power supply interface. The digital reference value is converted and sent as an electrically isolated analog reference to the power supply. After a predetermined delay to allow for settling times of interface electronics the timing controller orchestrates the acquisition of analog readback parameters and status information from the power supply. The acquired values are digitized and then sent back to the power supply controller as shown in figure 3. Corrector power supplies are not necessarily switched off during machine maintenance and monitoring is required. In the absence of reference update stream for periods exceeding 0.4 seconds, the power supply interfaces go into a second mode of generating status information continuously at a 10 khz rate for the LEB (1 khz for all other machines). This mode is also activated in case of link failure.

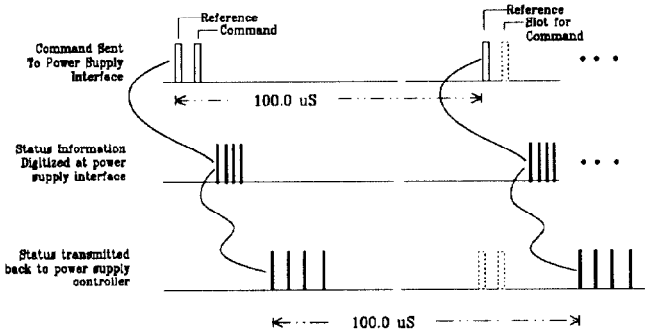

Figure 3: Corrector PS Controller / Interface Data Flow

The protocol for the 'DC' power supply controls is similar except that the reference values are sent to the power supply infrequently, usually at multiples of a 0.1S interval. The status information required for monitoring power converter performance is required to be readback at a 1 khz rate and is

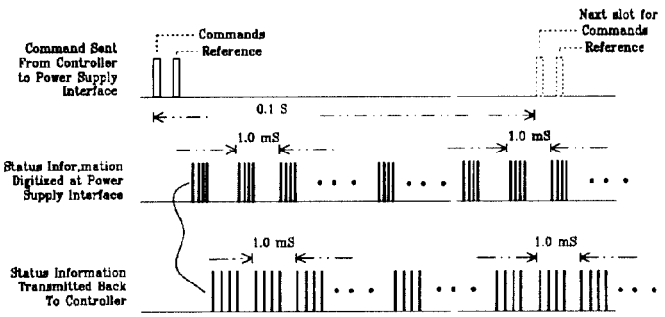

Figure 4: 'DC' PS Controller / Interface Data Flow

generated asynchronously as shown in figure 4.

The application level protocol format consists of fixed length, byte serial frames with a type field, indicating command or data, followed by one or more data fields. Commands are identified by a one in the most significant bit position and data by a zero. The following two bits identify the power supply types. The last five bits specify command number. All analog values are transferred as 16 bit values. Bipolar data is sent as sign plus 15 bit magnitude.

B. Link Level Protocol

Link level framing is asynchronous 8 bit plus parity with one start bit and one stop bit. Maximum intra frame byte separation allowed is 51.2 μS or 256 bit periods. Link state is initialized on time out. Explicit link management commands such as link initialize have not been specified in order to keep the link simple. For the slowest controller processor this corresponds to 512 instructions. This requirement is very easy to meet for the power supply interface electronics.

C. Physical interface

The physical interface between the power supply controller and the power supply interface is a bi-directional, bit serial, digital fibre optic link. The interface specification details media and optical signalling levels based on required Bit Error Rates (BER) as discussed later. A digital fibre optic link was chosen for the usual reasons of common mode isolation and immunity to electromagnetic interference.

A Total Output Deviation (TOD)[6] tolerable for power supplies is specified based on machine operation requirements. A digital interface allowed us to allocate a small, predetermined part of the TOD set by quantization error due to selected data word length or resolution in the controller. The rest of the allowable TOD is available to the power supply electronics. Problems of controls ADC / DAC drift and noise pickup are reduced. Location of error source is easier.

The Link encoding is bi phase mark. This is a modification of the bi-phase encoding used for the Fermilab machine data transmission link[7]. The mark condition corresponds to a fibre optic transmitter LED off condition and purports to lengthen the LED lifetime. Encoder and decoder implementation requires very few components and present strategy is to use popcorn logic followed by encapsulation using Field Programmable Gate Arrays.

III. ERROR DETECTION AND CORRECTION

A. Link Level

At the link level, an analysis was done about the expected number of errors under normal operating conditions for the 'DC' and the corrector magnet power supply. Fibre optic link BER depends on the optical loss budget and the receiver SNR. Using calculated BER of 1 in 10**12, expected errors for the 'DC' controller were about 1 per 300 shifts - with a shift defined as a 14 day running period. This was considered low and as such explicit error detection and correction in hardware was not felt to be necessary and was not planned to be done initially.

The link BER will be monitored on-line for link fibre optic component characterization and for failure prediction[4]. This is to address the combined 6.5 day MTBF of the ~24,000 fibre optic link components to be used on site.

Additional error sources are power supply and coupled noise in the controller and the power supply interface, the serial to parallel (and vice versa) conversion and the encoding / decoding done at each end of the link. End-to-end and link measurements to characterize actual BER achieved are therefore required to estimate actual errors expected.

B. Application Level

At the application level, effect of link errors on power supply operation need to be considered. Misinterpretation of Commands due to link errors can cause unacceptable down time for example by turning off a power supply which may then require some time for orderly turn on.

Given the calculated link error rates the command format encoding for all power supplies, interfaces and controllers is double bit. The likely hood of adjacent double bit errors is expected to be orders of magnitude lower than single bit errors and need to be characterized.

The effects of error on the reference output values for the 'DC' and the corrector magnet power supplies are some what different. The DC power supply references are sent infrequently such as few times per second. The expected errors in this is low and can for the time being be neglected. For the correctors drastically different values will be filtered out by power supply compliance limitations. Additional checking in may be imposed, in controller firmware, to allow some fractional change based on past values. This detail is yet to be determined.

C. Loose Packetization

Error checking at the application level frames is intended to be defined as the method of 'loose packetization', as an extension of application level framing. This would be a computed checksum for a group of (variable length) frames bracketed by a start checksum frame command and an end checksum frame command with the checksum transmitted as two bytes of data. These techniques are to be developed and will become useful by the time they are required for collider operations.

IV. DISCUSSION

The choice of protocols is driven by a number of factors such as the SSC Global controls architecture and machine operational requirements. Details of the protocol are decided by a tradeoff between implementation cost, component and resources availability. All of the specifications are evolving. The first specification is for a group of about 70 LINAC 'DC' power supplies. Future refinements of the design will be based on experience with this set. Presently encoders and decoders are being designed, BER testing is being setup, and methods to implement measurement of BER during controller operation are being looked into. Prototype controllers are expected to be made by the summer.

V. ACKNOWLEDGEMENT

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