High Resolution ADC Interface to Main Magnet Power Supply at the NSLS*

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Abstract

Previous readings of DCCT were limited to 11 bits of resolution with large offsets and drifts, providing inaccurate data. The current design overcomes this limitation by using Analog Device's AD7703 20 bit serial output ADC to digitize the main magnet DCCT at the power supply, and transmit the data serially at 2KHz over to the VME controller.

I. *INTRODUCTION*

The new system was designed to interface seven main magnet power supply DCCT's for the X-ray ring, and eight power supplies for the VUV ring with their respective VME controllers. To prevent disturbance of the power supplies, each with its own carefuly balanced isolated DC supply, any signal leaving the power supply must be isolated. In addition, the distance between the analog signal source and the VME must be kept to a minimum.

The new approach satisfies the above criteria by digitizing the DCCT analog signal at the power supply and transmitting the digitized signal serially via an opto-isolator. On the VME side the received signal passes through additional opto-isolators and the serial data is converted to a parallel format. This method achieves isolation from the power supply source, high noise immunity of the transmitted signal, and insensitivity to cable length. It requires only a few wires for transmission, and eliminates ground loop noise in the VME.

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II. *DIGITIZER*

The main components of the digitizer are the input instrumentation Amplifier (AD620), a precision reference (LT1019-2.5) and a 20 bit sigma delta ADC (AD7703). The ADC is a sigma delta converter which has a built-in 6 pole low pass gausian filter. The cut-off frequency is a function of the ADC crystal clock input. With a 2Mhz clock, the cut-off is set to 5 Hz and the rejection at 60 Hz is 90dB. The output of the ADC is in serial format: clock signal, data signal and a ready signal. This format interfaces directly with shift registers without additional hardware. In the circuit these outputs are first opto-isolated, then buffered through a differential line driver. Figure 1 shows the block diagram of the digitizer box.

The ADC can be self-calibrated by raising an input bit. The self calibration procedure measures the ground potential and the reference level, and recalculates the gain coefficient which is stored in the ADC. The ADC is configured to operate continuously, with a transmision rate of 2KHz.

In the implimentation of the circuit, high precision resistors with low temperature coefficients were used to set the gains. No potentiometers were used, thus rendering the circuit very stable. Each channel was calibrated and the slight offset and gain were corrected in the VME software. Calibration is effected by injecting a precise voltage source to the ADC inputs and modifing the coefficient in the computer data base to correct for any errors.

III. *VME BOARD*

Each VME board accepts 4 individual channels, where each signal first passes through an

opto-isolator. The clock and data signal interface directly with three 8 bit shift registers. The ready signal latches the output of the shift registers into three 8 bit wide latches. These latches are mapped as memory in the VME memory space. Since converted data is always available and updated in these memory locations, the VME can access the data at any rate any time. The whole ADC conversion is transparent to the VME and relieves the VME processor from the usual software overhead involved in interfacing with ADC's. The VME can initiate a calibration pulse to all the ADC's at any time, and freeze any update of the latches. The latter is needed when the VME accesses the full 20 bits of data. Since the VME data bus is set to 16 bits, two READ instructions are needed to access the full 20 bits.

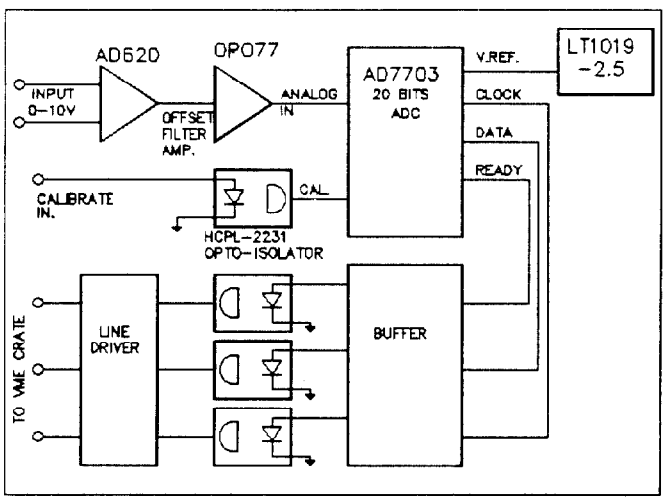

Figure 1. Digitizer block diagram.

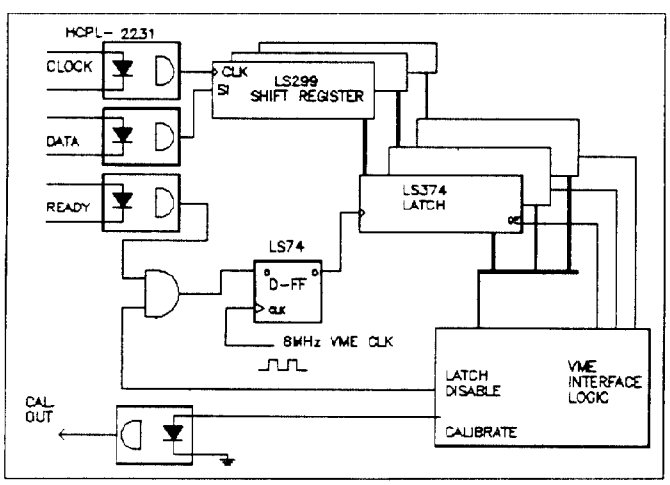

Figure 2. VME block diagram

IV. *RESULTS*

All units were built and installed and when calibrated showed an offset on the order of a few millivolts (out of 10 volts) and less then 0.5% gain variation from the desired nominal gain. A bench test of the ADC units showed better then 18 bits RMS noise (Figure 3). During operation, the set points to the power supplies are set by 16 bit DAC's. Although the readbacks contained 20 bits, only 16 bits have been displayed thus far. When the set points were compared with the 16 bit readbacks, in most of the supplies the two readings agreed across all 16 bits, (excluding some small fixed offset). In some readbacks jumps of only two bits were noticed.

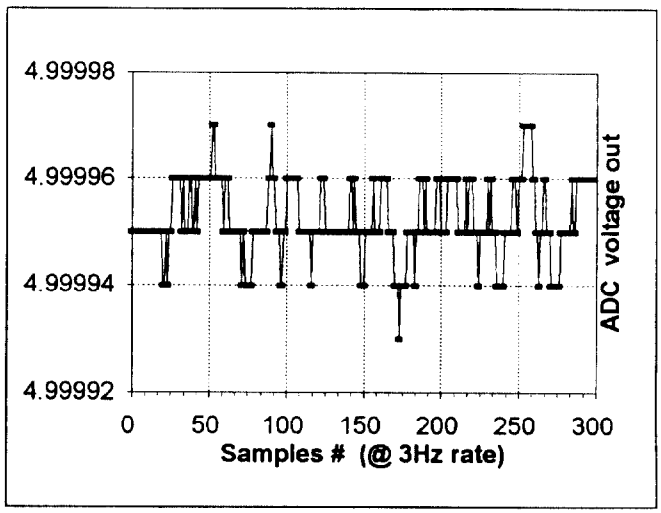

Figure 3. Noise measurement. Input to ADC is 5V.

V. *CONCLUSION*

The upgraded system is simple and cost effective, where the most expensive ADC IC is less than $25. The interface is very flexible (i.e. the VME board can accept any 24 bit data stream) and immune to noise and cable length. [With stable and repeatable read backs, comparison between DCCT readings and Hall Probe readings, could show hysteresis effects in the magnets.]