Anatomy of a Control System; A System Designer's View*

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Abstract

The ADVANCED LIGHT SOURCE (ALS) control system is quite unconventional in its design and implementation. This paper will discuss the system design considerations, the actual implementation, hardware and software costs, and the measured performance across all layers of the system.

I. INTRODUCTION

Three interrelated factors continue to drive accelerator control system design. The first is the ongoing evolution of semiconductor technology leading to rapid improvements both in speed as well as density of processors and support circuitry. The second is the ubiquitous presence of the personal computer (PC), the third is the revolution in software due to the large installed base of PC-s.

[1] As silicon systems continue to shrink in size and increase in speed and complexity, concepts that would have been prohibitive a few years ago are quite feasible now. A device controller that might have taken a half a rack in the 1960-s, a large chassis in the 1970-s, a VME or Multibus crate in the 1980-s can now be handled by a single 3U high Eurocard. This allows us to consider, once again, the viability of building, rather than buying, device control hardware.

[2] On the computer front, the downsizing of mainframes, minicomputers and workstations continues. While this downsizing has resulted in PC-s becoming a commodity item, it also has led to increased competition among manufacturers. Only the most efficient, large volume producers and those capable of extremely fast design cycles (to keep up with the rapid changes in processor technology) are able to survive due to the large investments required for R/D and fabrication facilities.

[3] A similar trend is now developing in software. Software is finally entering the phase where proprietary and expensive operating systems and large custom programs will not be viable. Very large volume sales will be required in order to sell software for low prices and at the same time afford the cost of development. (i.e. database prices that used to be > $1000 are now in the $100-s range).

I felt these three items were far more important than the peripheral issues (such as the 8086 vs. 68000, RISC vs. CISC, or minicomputer vs. PC) that dominated when we began construction. Therefore, in doing system design, after assessing the functional and performance requirements of the ALS (taking into account budgets and schedules), I tried to anticipate the impact of the three items above on the control system. This is particularly important on the software side, since an increasing fraction of control system costs and manpower goes toward software, often leading to cost over-runs and excessive staffing requirements.

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The resultant system architecture is shown in fig. 1; detailed description of system functionality and implementation is documented in refs. 1, 2 and 3. The device control level (layer 1) controls the accelerator devices while layers 2 and 3 connect device control and the operator interface (layer 4). Layer 5 is for the networking and development resources.

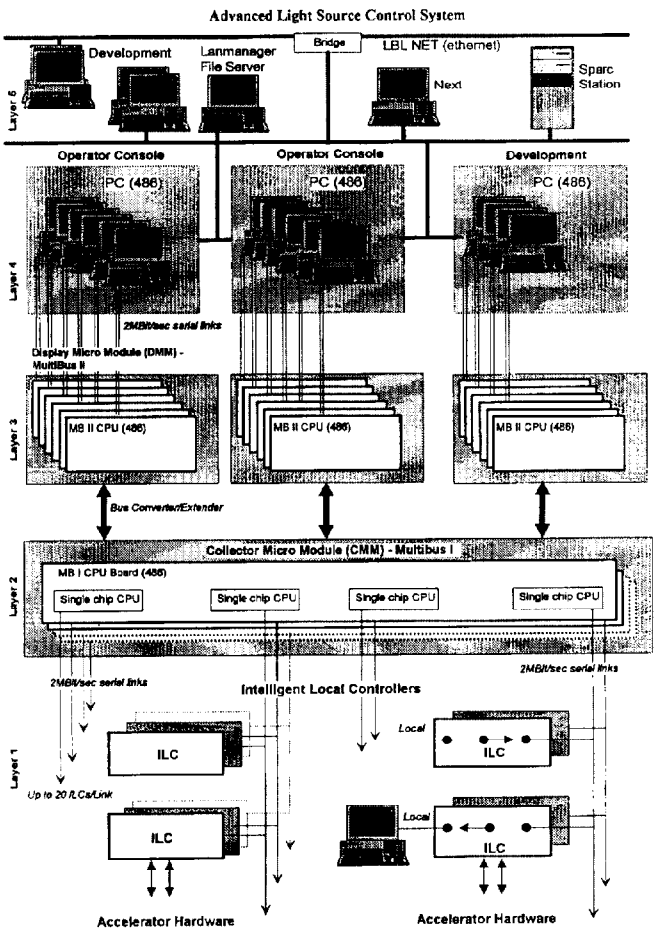

Figure 1. ALS Control System Architecture

II. SYSTEM ARCHITECTURE

A. *Distributed Device Control (Layer 1).*

The conventional ("bus" based) approaches to the device control problem was either to have a VME/Multibus chassis to which the signal cables are dragged from a large number of devices, or to have STD/Gespac crates (connecting to a few devices) communicating with VME/Multibus systems. I chose an approach which has the benefits of the STD/Gespac without the need for VME/Multibus; the result is the Intelligent Local Controller (ILC, see fig. 2). Designed at LBL (manufactured by outside vendors) it is an evolutionary step toward the single chip (or at least a few chip) solution. Such a custom controller was

economically feasible only if we could find a significant commonalty among the control requirements of the accelerator devices (power supplies, Beam position monitors (BPM), vacuum devices, oscilloscopes, etc.) so that ILC-s could be built in volume and thereby recover the development costs. At the same time I wanted functional advantages that would result in overall reduction in system/maintenance costs over the alternate "bus" based solutions. These advantages are: reduced cabling (a costly item) leading to a cleaner installation (fewer trays, less wiring to document), device control isolation and local control (since one ILC is responsible for one device, failure analysis is simple), control built into devices (smart instruments such as a BPM), and flexibility in device/controller placement. The ILC-s also eliminate the need for multi-card systems (and their noise sensitive digital buses) while providing better analog signal handling (lower noise) by allowing placement next to or in the device to be controlled. Power consumption is a mere four watts, resulting in reduced chassis power and cooling requirements, and sufficient computer power is built into the ILC so it meets the performance requirement of any device it controls.

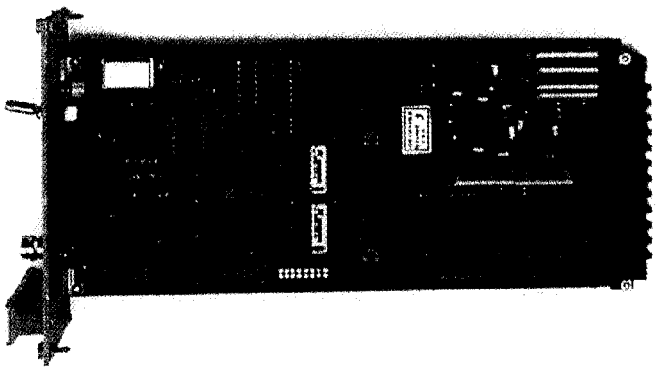

Figure 2. ILC

Two generations of ILC-s were built (175 of version I, 500 of version II), with respective costs of $650 and $1000. The added cost of version II is due to the resolution (nominally 16 bit) of the A/D converters, larger memory size and higher performance. Currently 400 ILC-s operate the accelerator; at full system implementation 500-600 ILC-s will be in use.

B. Communications (Layers 2,3).

When we began construction, the communication part of most control systems was handled by a few Token Ring or Ethernet based links. I chose a "star" type "shared memory" (the CMM, see figs. 1,3) approach to allow many parallel links to feed a centralized memory where data from many devices can be accessed quickly using a parallel bus. This type of "shared memory" system has the advantage that it can behave as a "router" (star-like routers are now coming into vogue for increased communications bandwidth) but in addition allows data to be "cached" for multiple access by a number of users without continually requesting data on the bandwidth limited links. Accelerator control systems are well suited to a "shared memory" architecture since data access is inherently asymmetric, i.e. for normal operation many devices need to be monitored by numerous users (increasingly by people in their offices), but few devices are allowed to be controlled .

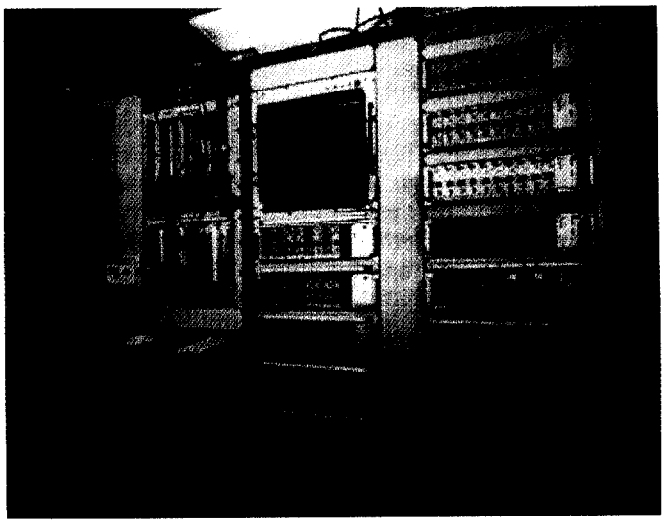

Figure 3. CMM, DMM-S, and Fiber Optic Links

Each of our currently installed 41 links runs at 2 Mbits/sec, for a total communications bandwidth of 82 Mbits/sec. The CMM has 7 CPU-s to support the links, with an expansion capability for up to 11 CPU-s to support 88 links. About 1400 data (average of 80 bytes) packets/sec are transmitted on each link. This amounts to an average of about 15 updates/sec of the active part of the entire accelerator database. The need for these high performance links is driven by the nature of distributed device control that de-emphasizes processor bandwidth with a concomitant increase in communications requirements. A control loop that used to be contained in a single chassis (VME or Multibus) now may be spread over a dozen device controllers; therefore the problems of feedback loops migrate from being a CPU performance issue (in a bus based system) to a communications issue among distributed device controllers.

The high communications bandwidth ensures that we meet the performance and deterministic response requirements of the feedback loops. Determinism means that data access is strictly a function of the number of links, devices on a link and the packets/sec/link and not dependent on user driven (i.e. what is being displayed on a console) system load. The need for determinism also led to a communications system that, rather than being message driven (conventional approach), is instead controlled by data update needs that are prioritized at the device (i.e. ILC) level. Since communications is often the limiting factor with many commercial devices (i.e. IEEE-488 link to a scope, or RS-232 link to a stepper motor), we want to limit data traffic to those devices, especially if multiple users want (often simultaneously) the same data.

For very fast data transfer, ILC-s can additionally communicate with each other directly up to about 2000Hz. This should be sufficient for the fast feedback loops that are expected to require a rate of about 200 Hz.

The DMM-s (see figs. 1,3), which access the shared memory, can act as a database, task or "permission" server for the operator stations. The DMM-s, using the "shared

memory" deterministic behavior of the CMM, can also act as a timing synchronization system. Since all the data arrives and leaves from one central location, it is possible to software synchronize the ILC-s without resorting to hardware timing signals. For the ALS a clocking system of 50 Hz could be done entirely in software, saving additional cost by eliminating the need for a hardware based timing and event tagging system. We used a software event tagging system, combined with a simple hardware interrupt distribution, to synchronize data access to 96 BPM-s from the operator station (PC-s). Such synchronization could be even faster if the software was executed in the DMM-s, where access to the data is at MULTIBUS bandwidth speeds.

C. Human Interface and Network. (Layers 4,5)

At the time of conceptual design, the most controversial part of the control system was the use of PC-s as the operator station (see fig. 1).

However, with the huge numbers of PC-s installed world wide (> 150 million) and the success of WINDOWS (30 million copies, and growing at the rate of 1 million/month), my prediction has paid off. With the imminent arrival of WINDOWS NT even large modeling applications can be accommodated. All of our current 16 bit applications already run unmodified on a beta version of WINDOWS NT (after writing a hardware interface Dynamic Link Library) with no change in the look and feel of the operating environment. The ubiquitous presence of WINDOWS has resulted in a rapidly exploding field of development tools (Visual Basic, Turbo Pascal for Windows, Visual C++, Toolbook, etc.) in addition to a large number of commercial applications (Designer, Excel, Word for Windows, Access, etc.). With the large sales volumes involved, prices of this software is rapidly declining (approaching commodity pricing) while features (Object Linking and Embedding [OLE], multimedia support etc.) and ease of use increases. This has resulted in a system to which many different individuals could contribute, depending on the level of their programming experience, thereby breaking the stranglehold imposed by systems that require "professional" programmers exclusively.

We use two dedicated links (identical in hardware to the CMM to ILC link) from each PC to communicate with a matching CPU in the DMM.; we achieve 1250 database accesses/sec for each PC. This currently is limited by processor speeds in the PC and the DMM; the link bandwidth will limit us to a maximum of 3000 accesses/sec/link. The 15 PC-s currently in use allow an aggregate of about 18,000 accesses/sec; however this is still a small fraction of the bus bandwidth that the CMM/DMM have available. When the Storage Ring was brought on line no degradation occurred in the data access to the existing parts of the accelerator. The PC-s can be upgraded to "PENTIUM" based systems thereby giving workstation ("RISC") like performance to the operator stations and even higher data access rates.

A conventional Ethernet interface (layer 5) allows the PC-s to communicate with a file server, workstations and other networked computers. We have provided for Remote Procedure Call based access to the database by UNIX based workstations (SUN, NEXT, IBM RS 6000). We note that recently many UNIX (and even Mac) based manufacturers are porting their operating systems to PC-s, as well as trying to provide WINDOWS compatible emulators, but with the arrival of Windows NT on the PC-s, workstations will not be required (they were needed for the large modeling applications that were too large for WINDOWS).

III. SCHEDULE, COST, STAFFING AND FUTURE OPTIONS

Over a period of 4.5 years $4.8 million (estimated escalated cost at beginning of construction was about $5.3 million) was spent on the control system. Of this cost, about 35% was for hardware, the remainder went for manpower (primarily software development) costs. An average of 5 people were required during the construction period; this includes software, coordination and management. The control system was on schedule and at no time delayed commissioning in any significant way, and can be maintained (due to its modularity) and software improvements added (for the currently needed functionality of the ALS) with a minimal staffing requirement of about 2 FTE-s.

The specifications, set out at the beginning of construction, have been exceeded in every category. The ILC-s are faster, more accurate and consume less power than anticipated; the CMM can handle more CPU-s and links. More DMM-s are in use than promised, and the PC front ends are more powerful and versatile.

Future improvements could complete the transference of WINDOWS based applications to WINDOWS NT, use network Dynamic Data Exchange to integrate application behavior among the many PC-s, and use OLE to allow an object based approach to application use and interaction. When Futurebus+ based systems become readily available, one could consider using them to replace the DMM/CMM. The use of an ATM or SONET based fiber optic system for the serial communications would allow replacement of the many parallel links with a single cable.

IV. ACKNOWLEDGMENT

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