

# PLL Subsystem for NSLS Booster Ring Power Supplies\*

J. Murray

Electrical Engineering Department, SUNY at Stony Brook,  
Stony Brook, NY 11794-2350, USA

R. Olsen, J. Dabrowski

National Synchrotron Light Source, Brookhaven National Lab  
Upton, NY 11973, USA

## Abstract

A high-performance digital phase-lock loop subsystem has been designed as part of the upgrade to the magnet power supplies in the booster ring at the National Synchrotron Light Source. The PLL subsystem uses a dedicated floating-point digital signal processor to implement the required filters and the startup, fault-handling, and running logic. The subsystem consists of two loops; the first loop tracks long-term changes in the line frequency, while the second tracks more rapid variations. To achieve the required performance, the order of the loop transfer functions was taken to be five, in contrast to the second- or third-order loops usually used. The use of such high-order loops required design techniques different from those normally used for PLL filter design. The hardware and software elements of the subsystem are described, and the design methodology used for the filters is presented. Performance is described and compared to theoretical predictions.

## I. INTRODUCTION

Output voltage control of high-current power supplies is usually based on the firing of thyristors at the appropriate phase-angle of the rectified A.C. line voltage. For this reason, accurate control requires a phase-reference which is accurately synchronized to the line over its range of frequency variation ( $\pm 0.1$  Hz); this is typically provided by a phase-locked loop (PLL) driven by the A.C. line. As the accuracy requirements of power supplies become more stringent, the performance demands on the PLL increase correspondingly.

To address this need, a high-accuracy digital PLL has been designed as part of the upgrade to the NSLS booster magnet power supplies. The design is based on the digital PLL previously used in this application [1]; in addition, to achieve the required performance, it was decided to use a relatively inexpensive floating-point digital signal-processing (DSP) chip, the Texas Instruments TMS320C31, to implement the required filters.

Since the design of DSP-based filters for PLL use is substantially different from that of analog filters, and the use of a signal-processing chip promotes a different design approach, the main emphasis in the following will be on the design of these filters.

\*Work performed under the auspices of the U.S. Department of Energy under contract DE-AC02-76CH00016

## II. PLL HARDWARE

### A. Overall System

A block diagram of the overall PLL subsystem is shown in figure 1. The core of the system is the block labeled "Fast Loop"; in normal operation, this provides the required phase-reference signal. The slow loop's function is to provide a relatively constant reference for short-time variations in the line and the fast loop; this is used mainly for diagnostic and measurement purposes. A secondary purpose is to provide a reference to which the fast loop can switch when the line fails.

It was decided, rather than attempting to provide multiple samples per cycle of the line phase, which would be sensitive to the purity of the line voltage, to use only a measurement of the length of each cycle. Since this is sensitive to noise in the zero-crossing region, the prefilter is used to provide a clean 60 Hz squarewave as input to the loops.

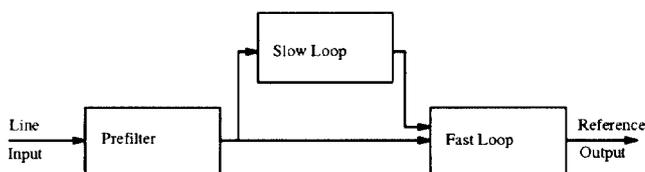


Figure 1: PLL Subsystem Block Diagram

### B. Fast Loop

The fast loop follows the usual PLL configuration; a block diagram is shown in figure 2. The digital VCO is essentially an overflow adder driven by a 23.592960 MHz crystal-controlled clock, and configured so that the output frequency is linearly proportional to the 20-bit input value, with an output frequency of 5.898240 MHz at midrange input, and a maximum frequency deviation of  $\pm 737.28$  kHz at inputs of 1 and  $2^{20} - 1$ . The frequency divider divides by 98,304 to give a center output frequency of 60 Hz, and a deviation of  $\pm 7.5$  Hz. The phase comparator consists of a 20-bit counter clocked at 10 MHz; this gives a resolution of .002 degrees.

### C. Slow Loop

The slow loop is similar to the fast loop except for the following: 1) the VCO is a voltage-controlled crystal oscillator, with the control voltage set by the output of a

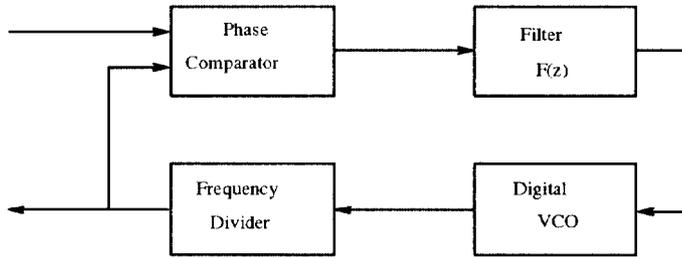


Figure 2: Fast Loop Block Diagram

16-bit D/A converter; 2) since this gives a very low frequency range, the frequency divider is also made variable to increase the range. This arrangement was chosen to achieve extremely fine resolution for VCO, since the time-constant for the slow loop is of the order of hours.

### III. PLL FILTER DESIGN

#### A. Loop Requirements

The main requirements were for acceptable acquisition time (not more than a few seconds), asymptotic tracking error of better than .02 degree across the frequency range 59.9-60.1 Hz, and good rejection of noise, harmonic distortion (120 Hz up); and disturbances induced by the power supply ramping itself (25 Hz down).

Since a DSP chip is being used, low order is *not* a requirement. This makes the “coprime fractional representation” approach to feedback design [2] very attractive; the version used here is taken from [3].

#### B. Fast Loop

Since the phase difference is sampled at the end of each cycle, and gives the average phase difference over that cycle, the transfer function of the VCO and frequency divider, as seen by the filter, can be modeled as

$$P(z) = \frac{Kz^{-1}}{1-z^{-1}}$$

where  $K$  is a hardware-dependent gain. The phase-comparator is simply a difference operator followed by a gain  $K_d$ .

The problem then becomes: find a filter  $F(z)$  which stabilizes this loop, asymptotically tracks a ramp input, and rejects noise and disturbances. Tracking of a ramp input is required since a step change in frequency is a ramp in phase, and asymptotically zero phase error is desired over the frequency range.

Following the method in [3],  $P(z)$  is first expressed as a quotient  $n_p/d_p$ ; in this case  $n_p = Kz^{-1}$  and  $d_p = 1-z^{-1}$  are natural choices. The pair of functions  $u_p = 1/K$  and  $v_p = 1$  is then chosen as a solution for the equation (2.15 in [3])

$$u_p n_p + v_p d_p = 1$$

Next, since the Z-transform of a ramp is  $z^{-1}/(1-z^{-1})^2$ , the functions in equation 3.2 in [3] can

be taken to be  $n_t = z^{-1}$ ,  $d_t = (1-z^{-1})^2$ ,  $u_t = 2-z^{-1}$ , and  $v_t = 1$ .

In a similar way, the functions  $u_{pt}$  and  $v_{pt}$  in equation 3.14 in [3] can be taken to be  $(2-z^{-1})/K$  and 1, respectively, and the functions in equation 3.28 in [3] can be taken to be  $n_a = 1$ ,  $d_a = 1-z^{-1}$ ,  $u_a = 1$ , and  $v_a = 0$ .

It then follows from the theory presented in [3] that, for *all* stable functions  $\epsilon(z)$ , the filter

$$F(z) = \frac{1}{K_d} \frac{-e(z)d_a d_p + d_p v_p u_{pt} + u_p}{e(z)d_a n_p - n_p v_p u_{pt} + v_p} = \frac{1}{KK_d} \frac{-Ke(z)(1-z^{-1})^2 + 3 - 3z^{-1} + z^{-2}}{Ke(z)z^{-1}(1-z^{-1}) + (1-z^{-1})^2} \quad (1)$$

will give a stable closed-loop system which will track a ramp input, and that *all* such filters are of this form. Further, the gain from the input to the sampled output is given by

$$H(z) = \frac{-e(z)d_a d_p n_p + d_p v_p u_{pt} n_p + u_p n_p}{1 - (1-z^{-1})^2(1-z^{-1} + Ke(z)z^{-1})} \quad (2)$$

which is linear (more accurately, affine) in  $Ke(z)$ . The arbitrary stable function  $Ke(z)$  can therefore be taken as a free parameter to optimize the other requirements. In this case,  $\epsilon(z)$  was taken to be a general second-order stable transfer function, and the coefficients were chosen to give a low-pass characteristic with good rejection at 2 Hz, which is the ramp frequency of the final system [4]. The filter transfer function for this weighting factor was found by substituting this  $Ke(z)$  in equation 1; the result was

$$F(z) = 0.92262464 \frac{3 - 3z^{-1} + z^{-2}}{1 - z^{-1}} \times \frac{1.022612 - z^{-1}}{1 + .29733659z^{-1}} \times \frac{1 + z^{-1}}{1 - .31896065z^{-1} + .072725713z^{-2}}$$

which was implemented in cascade form.

#### C. Slow Loop

The procedure for the slow loop was identical except for the loop constants and the weighting factor; the latter was chosen so that the 3-dB point of the PLL frequency response was about  $6 \times 10^{-5}$  Hz, corresponding to about 4.6 hours response time.

#### D. Prefilter

The problem with the prefilter was to design a band-pass filter with approximately *constant* phase across a small region in the middle of the band. This was achieved by first satisfying the condition at 0 Hz in the analog domain, using a frequency transformation to transform to a bandpass filter, and a bilinear transform to transform to the Z domain. More specifically, since phase and amplitude matching was required at DC, and a second-order

rolloff at was desired at high frequency, the transfer function of the prototype filter had to take the value 1 to the second order at zero (assuming unity gain), and had to have a second-order zero at infinity. This led to the form

$$H_a(s) = \frac{a_1 s + a_0}{s^3 + a_2 s^2 + a_1 s + a_0}$$

and the values  $a_0, a_1$ , and  $a_2$  were determined by iteration. After the lowpass-to-bandpass and bilinear transformations, the following sixth-order filter was obtained (in cascade form):

$$H(z) = \frac{6.9980052 - 13.976087z^{-1} + 6.9880187z^{-2}}{1 - 1.9965836z^{-1} + 0.9980031z^{-2}} \times \frac{5 \times 10^{-6}(1 - z^{-1})^2}{1 - 1.988673z^{-1} + 0.99008866z^{-2}} \times \frac{(1 + z^{-1})^2}{1 - 1.9886052z^{-1} + 0.99001764z^{-2}}$$

## IV. PERFORMANCE

### A. Predicted Performance

The calculated amplitude response for the fast loop is plotted in figure 3; its 3-dB frequency is .6 Hz. By design, the filter is stable, and has zero asymptotic tracking error for a ramp input.

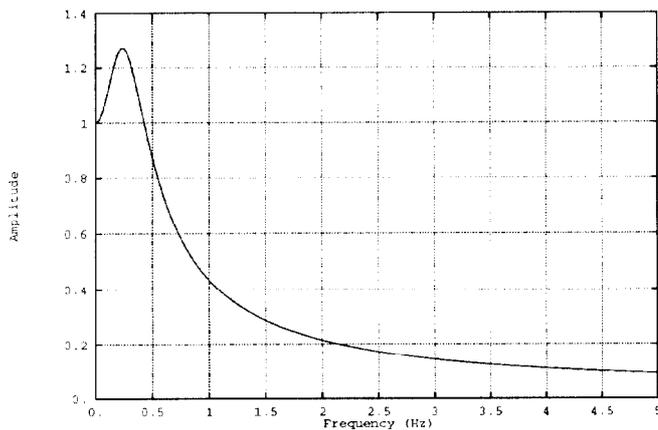


Figure 3: Fast Loop Amplitude Response

The calculated amplitude response for the prefilter had a bandpass characteristic with 3-dB points at 53 and 67 Hz, and had an attenuation of > 27dB below 30 Hz and above 120 Hz.

Finally, the prefilter phase response for the range 59.9 – 60.1 Hz is shown in figure 4; the maximum phase deviation over the band of interest is less than  $\pm 0.01$  degrees.

### B. Measured Performance

The prefilter and the remainder of the PLL system were implemented separately.

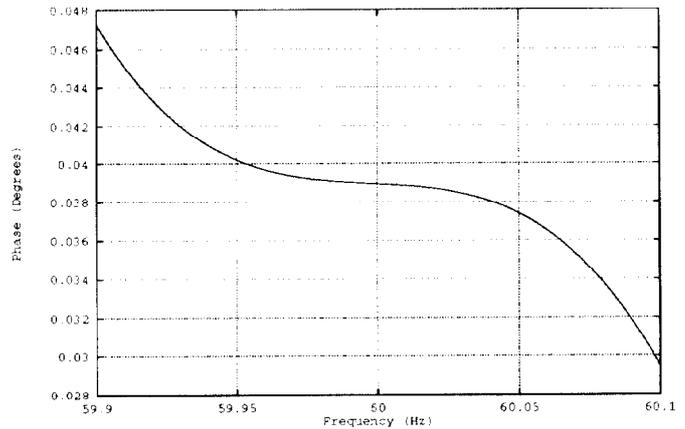


Figure 4: Prefilter Phase Response

The prefilter was implemented on the Texas Instruments TMS320C30 EVM board, and was tested with a function generator as input. Within the limits of measurement error, it functioned as predicted.

The remainder of the PLL system was implemented on a VME-bus system, controlled by a VME-based TMS320C30 board; the algorithm included all initialization, status, error condition handling, and the loop filters. The measured steady-state ramp tracking error was 0 across the frequency band (within the resolution of the phase detector) when the input was taken from a bench function generator.

Because of the long time-constant, precise measurements of the slow loop were not possible; however, it functioned as expected, and had an extremely long response time. The lock-in performance of the fast loop is so good that the slow loop will be necessary only for measurement and diagnostics.

## VI. REFERENCES

- [1] R. Olsen, "A High-Performance Digital Triggering System for Phase-controlled Rectifiers," Proceedings 1993 IEEE Particle Accelerator Conference, March 21–23, Santa Fe NM, p.2867
- [2] D.C. Youla, J.J. Bongiorno, and H.A. Jabr, "Modern Wiener-Hopf Design of Optimal Controllers: Part I," *IEEE Trans. Autom. Contr.*, Vol. **AC-21**, 1976, pp. 3–15.
- [3] R. Saeks, J. Murray, O. Chua, C. Karmokolias, and A. Iyer, "Feedback System Design: The Single-Variate Case — Part I," *Circuits, Systems, and Signal Processing* Vol. 1, No. 2, 1982, pp. 137–169.
- [4] R. Olsen, J. Dabrowski, and J. Murray, "Control System for NSLS Booster Power Supply Upgrade II," these proceedings.