# Possibilities and Limitations for a Fully-Digital RF Signal Synthesis and Control

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### Abstract

Since the advent of VLSI circuits capable of data rates in excess of 30 MWords/s, real time digital rf synthesis has become an interesting and viable avenue to be used with accelerators. This technique builds up rf signals from a real-time sequence of digital words with minimum use of analog components. With digital rf, hitherto not achieved agility, precision, and reproducibility for frequency and phase are now possible. This permits optimum acceleration ramp functions, subject to any desired constraints in longitudinal phase space. as given phase or voltage or acceptance, or yet another bucket quantity. Since phase fidelity is crucial with accelerator applications, a high degree of over-sampling is mandatory, posing the only actual limitation to these new techniques. However, with clock rates of more than 1 GHz, today's component technology limits the rf carrier to some ten to about 100 MHz, depending on which signal-to-noise ratio is acceptable. This range can further be extended by means of analog up-conversion. A number of digital rf techniques have been developed at the COoler SYnchrotron COSY, e.g. for rf acceleration and ultraslow extraction, and were made available also for the acceleration with TSR, Heidelberg. Further possible applications are being explored.

### 1. INTRODUCTION

Acceleration systems in synchrotrons commonly consist of (current-biased) ferrite loaded cavities, controlled by a phaselocked loop (PLL) type tuning control, a high power amplifier, a low-level variable-frequency oscillator, and a beamphase to gap-voltage phase feedback, again of PLL type.[1] The associated frequency signals, and also the control loop signals are commonly generated and manipulated by analog methods, mainly by mixer circuits, and by voltage controlled oscillators (VCO), to accommodate the large frequency swings of up to a factor of ten. To overcome the inherent drawbacks of VCOs, like their lack of absolute accuracy and stability limitations, specifically, their hystereses in output frequency, digital synthesis methods are now being used more and more. since very large system integration (VLSI) in circuits for this end have emerged on the market. While many of these synthesis methods had been thought of, and, at some instances, used since several years in hybrid circuits, only today's availability of the compact VLSI components make direct digital synthesis (DDS) practical for the large number of variable frequency signal generation tasks common in synchrotrons. However, unlike DDS with audio applications, where digital signal processors can be used, DDS in the rf range must employ dedicated function circuits. To preserve phase fidelity,

moderate to high over-sampling is necessary, which essentially curtails the maximum carrier frequencies and/or signal-tonoise ratios, the latter being directly related to the digital value resolution (number of Bits).

### 2. DEDICATED-FUNCTION COMPONENTS

The major DDS building blocks are numerically controlled oscillators (NCO), multipliers (used for mixers or in filters), and converters from the analog signal world to the digital realm (ADC) and back (DAC). Characteristic performance values of such devices, which are commercially available at this time, are shown in Fig. 1.



Fig. 1: Performance of present day digital rf VLSI circuits

### 2.1. Numerically controlled oscillators

According to Fig.1, NCOs can generate frequencies, that typically are on the order of particle revolution frequencies (or their lower harmonics) in synchrotrons. Hybrid and up-conversion schemes with additional analog local oscillator frequency signals extend the range even more, or allow to further reduce spurious content. NCO techniques are thus well suited for generating frequency signals in synchrotrons, including frequency generation for beam diagnostics. [2]

Inside an NCO, a clock continuously advances by the increment  $\Delta \Phi$  a polar phase vector on the unit circle, passing on the corresponding projections as  $\sin(\omega t)$  and/or  $\cos(\omega t)$  computed via a cordic algorithm, or looked up from a table (LUT). Thus, the (synthesized carrier) frequency  $f=\omega/2\pi$  follows from this increment  $\Delta \Phi$ , given in N-Bit resolution, and the clock frequency,  $f_c$ , as

$$f = \frac{\Delta \Phi f_c}{2\pi (2)^N} \quad . \tag{1}$$

Equation (1) suggests two possibilities for varying the frequency f: Either one varies the phase increment, or one varies the clock frequency. The constant clock frequency is the usual approach. Choosing the clock frequency to be an exact harmonic will greatly reduce the LUT, and thus the NCO. It will improve signal to noise ratio to better than the "theoretical" 6.02dB/N. This shifts the task to the variable (programmable) clock, for which we used, for our applications, again the NCO principle. In any event, NCOs commonly outperform conventional rf generators in typical characteristics, as accuracy, stability, tuning range/bandwidth, resolution, tuning speed, and signal modulation capability. The reason for this is, that the NCO frequency is derived from a high clock frequency, whether fixed or varying. Phase noise stems essentially from the clock oscillator, and is, moreover, reduced due to the frequency down-division by the amount  $20\log_{10}f/f_c$  [dB]. Switching speeds are characterized by electronic on-chip delays, and not by a quality factor, as in analog oscillators. NCOs, together with the attached output DAC, are limited by their real-time "computing" and conversion speed, resulting, for practical applications, in carrier synthesis of up to 500 MHz at signal-to-noise ratios (or spurious levels) of 42 dBc, or better for lower clock (i.e. carrier) frequencies. On the other hand, frequency resolution of a fraction of a Hertz is no exception. Hybrid and up-conversion schemes with additional analog local oscillator frequency signals extend the range even more, or allow to further reduce spurious content. NCO techniques are thus well suited for generating frequency signals in proton or heavy ion synchrotrons, including frequency generation for beam diagnostics.[2]

#### 2.1. Modulation and demodulation schemes

As in the analog realm, digital rf signals can be amplitude, frequency and phase modulated. This is done either by direct modulation of the input values for frequency and phase, or by separate multiplication via a VLSI multiplier.[3] Amplitude modulation, if not critical, may be done by suitable gain control in the analog output stage. For correlated digital modulation of frequency, phase *and* amplitude, again a multiplier must be used, or two suitably phase-modulated NCOs with subsequent signal summing.[4] Again by means of digital multiplication, amplitude, frequency and phase demodulation is possible in quadrature, permitting, e.g., a full  $4\pi$  phase demodulation within only a few rf cycles.[3]

# 3. RAMP-FUNCTION SYNTHESIS [5]

One attractive possibility with a completely digital synthesis is the direct digital generation and input of RF acceleration ramping functions, without to resort to the analog realm. These ramping functions for frequency, rf voltage amplitude and (beam-to-rf) phase may be precisely computed beforehand, to take into account beam-dynamic evolution or constraints, as for instance, adiabatic cooling during the acceleration process. This suggests the continuous optimization of the longitudinal phase space available for the beam particles during the acceleration process. The direct digital synthesis of rf signals with high value precision has, thus, to face the issue of generating a rapid digital ramp input on a corresponding level of value precision, and, as a consequence, of temporal resolution.

#### 3.1. Frequency Law

Due to the velocity variation during acceleration in proton and heavy-ion synchrotrons, the rf frequency must be tuned along according to the temporal law for the particle momentum p(t), or synonymously, for the magnetic dipole fields.

$$f_{\rm rf}(t) = f_{\rm rev}(t) = \frac{f_{\infty}}{\sqrt{1 + \left(\frac{E_0}{cp(t)}\right)^2}} \qquad (2)$$

The revolution frequency for particles at speed of light is denoted by  $f_{\infty}$ , their momentum by p(t), and their rest energy by  $E_0$ . Especially the resolution needs for the frequency may be high, easily on the order of 24 to 32 Bit, while phase and amplitude may pose less demanding requirements. Note, that with a required frequency resolution  $\Delta f$  based on physics considerations, the associated requirement for digital value resolution, N Bits, follows the rule N +1 =  $\log_2 f_c - \log_2 \Delta f$ . With a resolution of N=20 or more Bits, a timing discretisation of some hundred nano-seconds may become necessary, in order to retain the intended resolution at all times, as can be shown generally (Fig. 2).[5] For a dipole field variation of 1 T/s, for protons and a frequency resolution of 10<sup>-6</sup>, the time step is about 1 µs. Today's fast memory banks, that can provide one 32-Bit data point in less than 100 nano-seconds for several seconds guarantee a precise ramp input. Real-time ramp value computation, based on rapid linear or quadratic inter- or extrapolation in between a sparser grid of ramp points relaxes the time step resolution for these ramp points somewhat, Fig. 2, but poses problems due to the slope quantization of the then needed digital accumulation procedure.[5]



Fig. 2: Frequency and time step resolution

### 3.2. Phase and amplitude law

The ramp functions for phase  $\phi_s(t)$  and amplitude  $U_o(t)$  are more involved, but may be computed generally for arbitrary rf.[5] They depend on the wanted particle energy increment per turn,  $\Delta(t) = U_o(t)\sin\phi_s(t)$ , and also possible constraints in longitudinal phase space. One relevant constraint, especially early into the acceleration, is the momentum acceptance  $\delta(t)$ of the bucket, that at no time should exceed the transverse acceptance of the ring. Only two of these temporal dependencies may freely be assumed; all others follow then directly from this choice.

# 4. BOARD-LEVEL DEVELOPMENTS [3,6]

For various tasks, as frequency signal generation, real-time filtering, ramp function generation, modulation and demodulation, real-time precision phase measurement and phase correction (0.1°/ 2MHz/5µs), programmable time varying clock signal generation (>100 MHz, 150 ps jitter), and the associated interfacing to accommodate these circuits within the VME/ VXI standard, we have developed a number of DDS boards. All these boards may be combined in various configurations, to achieve a wide variety of synthesis, measurement, control and feedback functions. Table I shows some of the boards' key features. Our systems, in various functions, have proved indispensable during acceptance and commissioning of the COSY rf acceleration station, and of the entire COSY ring. In addition, one system was made available for, and by now, was successfully used with acceleration experiments in TSR, Heidelberg. Similar plans exist for CRYRING, Stockholm.

function	f <sub>c</sub> [MHz] 1	N.of Bil	S	used for
NCO1	25	16	I+Q	frequ. synthesis
NCO2	90	12	I or Q	frequ. synthesis
NCO3	var.	16	I or Q	frequ. synthesis
DAC1	>100	12		signal synthesis
DAC2	>10	16		control loops
ADC	>25	12		measurement/control
Multiplier	>25	16x16		mixer, phase shifter
A-demod	>25	16x16		instant. ampl. demod.
Adder1	50	16+16		simple arithmetics
Adder2	90	12+12		amplitude modulation
Var.Clock	$1-1.6 \times 10^3$	8		phase control system
FIR-Filter	1 >25	16	2 <sup>4</sup> taps	phase control system
FIR-Filter.	2 >25	16	$2^{11}$ taps	phase measurement
(r,ø)<->(x,	y) >25	16		coord. transform.
Converter	1	20		ramp funct. synthesis

Table I: Some DDS boards developed by COSY-RF

# 5. FURTHER DDS APPLICATIONS

Other, more exotic applications are also studied, as the phase-correlated second and third-harmonic synthesis required for higher-harmonic drives to modify bucket properties, especially, when passing transition or for other beam pulse shape gymnastics.[7,8] With several NCOs, the phase-rigid (or

phase-corrected) and exactly frequency-tracking synthesis of higher harmonics is no problem. Another interesting method may be employed, when operating a truly wide-band rf high power structure, as does the new accelerator CRYRING.[9] Instead of standard harmonic signal generation via a look-up table containing trigonometric information, an arbitrary-value look-up table permits the time-varying synthesis of saw-tooth type signals, by which phase space may be maximized.

Finally, we have also embarked on the development of the digital signal synthesis for an ultraslow extraction system, where a beam coherent harmonic is to be superimposed with exactly tailored phase and/or amplitude noise, so as to modify the momentum distribution of the particle beam.[10,4] One appealing aspect of this is, that the digital synthesis of noise should permit a direct comparison with standard longitudinal particle simulations.

# 6. CONCLUSIONS

High-precision, fully digital rf frequency synthesis, phase control, and measurements for carriers up to tens of Megahertz have become feasible with the advent of modern VLSI circuits of high clock-rate capability. Moreover, some features impossible with conventional methods may now be tackled with these digital rf techniques. Due to their board modularisation, systems can be configured flexibly, and should be suitable for other accelerator applications as well. The limitations in clock speed and/or value resolution (i.e. S/N) pose the only true limit for higher frequency applications, although these limits are continually being pushed ahead with the availability of faster and faster circuits.

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