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# A FAST ENERGY DUMP FOR BEAM LINE MAGNETS

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## Introduction

Energy dump circuits have been used extensively for the protection of superconducting magnets and as such are low duty cycle devices. This paper describes an energy dump circuit specifically designed for high duty cycle use on conventional magnets up to 5000 amperes. This energy dump system was developed to permit rapid (to 10 ms) reduction in magnet current in high inductance conventional magnets on a pulse to pulse basis of the accelerator. The design, construction and operational characteristics of the system will be discussed.

## Basic Circuit Operation

Figure 1 shows the basic circuit schematic.

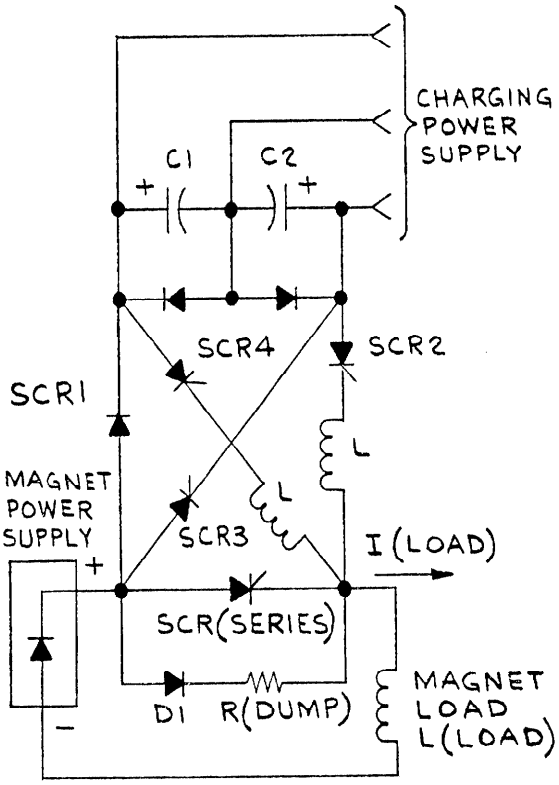


FIGURE 1

The magnet power supply is pulsed at the main ring period. The control circuit that regulates the operation of the fast ramp down circuit will initially charge Capacitor Bank 2 (C2) to 275 v dc. Gate trigger pulses to SCR (SERIES) permit the load current to rise to the desired level. At the time fast ramp down is initiated, the gate pulses to SCR (SERIES) are interrupted and a signal is sent to the magnet power supply to begin phasing back to zero output voltage. Then, for Bank 2 charged, SCR 1 and SCR 2 are triggered, shifting the load current through SCR 1, Capacitor Banks 1 and 2, and SCR 2. This reduces the current through SCR (SERIES) below its holding current and it then shuts off. Bank 2 discharges as Bank 1 charges. Current flows to Bank 1 and through D1 and dump resistor R(DUMP) until Bank 1 voltage equals (I Load) R(DUMP). At this time SCR 1 and SCR 2 shut off. The load current continues to flow through the load, D1, R(DUMP), and the magnet power supply free wheeling diode, falling at a rate determined by R(DUMP / L(LOAD). The ramp down circuit is now armed for the next pulse with Bank 1 charged. The small capacitor bank charging supply can make up voltage if the period of the cycle is long and the capacitor bank begins to discharge through other circuit impedances. After the load current has reached zero and before the main power supply is ramped on, SCR (SERIES) is again triggered to permit the load current through the load. The entire cycle is again repeated for the next cycle this time using Bank 1 charge, SCR 3 and SCR 4.

## Design Criteria

In considering various techniques to accomplish a rapid ramp down of inductive (magnet) loads, several factors were considered to arrive at this solution. The maximum ramp down (load) voltage permitted would be 1000 v. This was dictated by the type of magnets used at Fermilab, the cables used for connecting poser supplies and magnets, available components, and power supply capabilities. The value of R(DUMP) is determined by this criteria.

The "flip flop" arrangement reduces the total RMS currents in the capacitor banks and permits a lower power capacitor bank charging power supply. Also, only one additional SCR was needed to implement this scheme over a non-"flip flop" scheme.

Operational requirements required the construction of three versions of this basic circuit; 200A, 500A, and 5000A. Also, all circuits are to be controlled by the same control logic design, thereby limiting circuit differences to the ramp down circuit only.

## Circuit Analysis

A detailed analysis of the circuit of Figure 1 can readily be derived for each of the design cases, i.e., 200A, 500A, and 5000A. In summary, however, the most stringent condition exists at the moment of commutation. Again choosing the case of Bank 2 charged and SCR 1 and SCR 2 triggered. The circuit of Figure 2 applies.

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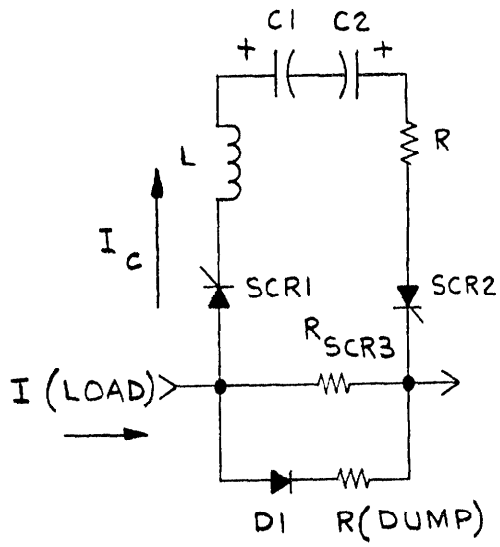


FIGURE 2

The transform for this circuit

$$L[sI_c - i(0^+)] + RI_c(s) + \frac{1}{C_1 s}[I_c(s) + q_1(0^+)] + \frac{1}{C_2 s}[I_c(s) + q^2(0^+)] = 0$$

where:

$i(0^+)$ = initial current flowing in L = 0

$R_{SCR3}$ = 0

$V_{OC1}$ = initial voltage on C1 = 0

$V_{OC2}$ = initial voltage on C2

I(LOAD) = magnet current

$I_c$ = commutation current

R = commutation circuit resistance

C1 = C2 = C

then from initial conditions:

$$q_1(0^+) = -C1V_{OC1} = 0$$

$$q_2(0^+) = -C2V_{OC2}$$

Simplifying and solving for $I_c(s)$:

$$I_c(s) = \frac{V_{OC2}}{L}\left[s^2 + \frac{RC}{L}s + \frac{2}{LC}\right]$$

Since Rc is very small, the particular solution is of the form,

$$i_c(t) = \frac{Vo}{KI}\ 1^{-K2t}\ \text{Sin K3t}$$

thus, $i_c$ increases as C2 discharges and C1 charges and then decreases to zero when C1 is charged to R(DUMP) I(LOAD). At this time SCR 1 and SCR 2 shut off completing the commutation cycle. It can be seen that C1 and C2 are chosen to insure a commutation current pulse duration longer than the turn off time of SCR (SERIES).

To insure long life to the commutating thyristors (SCR 1 and SCR 2), L is chosen to produce a di/dt within the thyristor specifications. Also, a fast rise (< 1 μs) high current (> 2A) trigger pulse is used for the commutation thyristors.

Further, it should be noted that the above analysis ignores the reverse current through SCR (SERIES) that flows until SCR (SERIES) shuts off. This current can be substantial and leads to choosing C1 and C2 to be somewhat larger than indicated by the calculations.

## Summary

Tests of the 200A and 500A versions show excellent agreement with calculations and have operated without incident for some time. A 5000A version of a slightly different configuration has functioned well for over six months. The introduction of the fast ramp down circuits has substantially increased the flexibility of the Neutrino beam line by permitting the effective use of the accelerator flat top.

## Acknowledgments

The author is indebted to Gary Ross, Karl Varga, Bill Williams and Chuck Worel. Each were involved in the construction and testing of the equipment and each contributed to the design and implementation of the system.

Acknowledgment of the parallel efforts in the design of ramp down circuits for superconducting magnets must also be made to John Dinkel, Age Visser, and John Stoffel; all of Fermilab.

A detailed analysis of the Meson Dump System can be found in John Stoffel's Technical Memo - Fermilab TM-835, December 1978.