IEEE Transactions on Nuclear Science, Vol. NS-26, No. 3, June 1979

A MICROPROCESSOR BASED BEAM INTENSITY AND EFFICIENCY DISPLAY SYSTEM FOR THE FERMILAB ACCELERATOR

Richard Biwer*

ABSTRACT

The Main Accelerator display system for the Fermilab accelerator gathers charge data and displays it including processed transfer efficiencies of each of the accelerators. To accomplish this, strategically located charge converters monitor the circulating internal beam of each of the Fermilab accelerators. Their outputs are processed via an asynchronously triggered, multiplexed analog-to-digital converter. The data is converted into a digital byte containing address code and data, then stores it into two 16-bit memories. One memory outputs the interleaved data as a data pulse train while the other interfaces directly to a local host computer for further analysis. The microprocessor based display unit synchronizes displayed data during normal operation as well as special storage modes. The display unit outputs data to the front panel in the form of a numeric value and also makes digital-to-analog conversions of displayed data for external peripheral devices.

DATA ACQUISITION SYSTEM

The major components of the data acquisition system consists of charge converters monitoring the circulating internal beam of each of the Fermilab accelerators, an asynchronously strobed multiplexed analog-to-digital converter and two 16 bit memories. The charge converters are located at the following locations: Linac (MH1), Booster (Long 20), Bim 10 (8 GeV), Bim 50 (8 GeV) and Main Accelerator (A17).

Service requests are sent to the data acquisition system for each of the above charge monitors. Each monitor output is digitized typically thirteen times for each main accelerator cycle. These requests are prioritized having Linac data the highest priority and the Main Accelerator the lowest. Once the charge data is digitized the channel address code is added and the newly fabricated sixteen bit data word is then stored in two local memories. After the data enters the local memories the data distribution system becomes active and distributes the stored data using two methods.

DATA DISTRIBUTION SYSTEM

The major components of the data distribution system consists of two sixteen bit memory output ports, a data pulse train generator and a full handshake interface to a local host computer.

One of the sixteen bit memories, outputs to a data pulse train generator which address decodes the interleaved data words and outputs the data to the appropriate output port. Data output continues until the memory empties.

The second sixteen bit memory accumulates the interleaved data and outputs it to a host computer using a full handshake technique.

This duo output method allows the user to accumulate the data remotely as well as inputing the data to a host computer for data logging, plotting and further analysis. Both memory units have separate output controllers allowing them to operate completely independent of each other.

BEAM INTENSITY AND EFFICIENCY DISPLAY UNIT

This display chassis resides in the Main Accelerator Operating Console and includes a stand alone microprocessor system. The system contains a maximum of six kilo-bytes of read-only memory, one kilo-bytes of random access memory and has eight levels of prioritized interrupts. Included in the system are special function printed circuit boards to route data efficiently during real time operation.

Front Panel

The front panel consists of numeric displays, control push button switches and a digital sense switch. Numeric data is displayed using numeric display modules mounted on the rear of the machined front panel and viewed through lucite display shields. Under software control, data is relocated from random access memory to the display panel using multiplexed display modules. These modules interface with the matrix oriented front panel numeric display modules. All displayed numeric characters are separately relocated from random access memory to a predetermined matrix address corresponding to each numeric display character position. Although data is programmed to be relocated to preassigned display locations, it can be altered to any display address by revising the software program. A photograph of the front panel shows additional construction details.

Controls

The control push button switches on the left side of the panel provide a means of selecting the mode of operation desired. These controls are labeled FPC (front porch control), stop, start, clear and TPA (ten pulse average). The following suggests some possible modes or combinations of modes used:

FPC - "Front Porch Control" is selected by the user when the main accelerator magnet program includes a magnetic plateau prior to the peak value or flattop. This control flags the system to measure the accelerated circulating charge prior to entering the plateau portion of the magnetic program. If FPC is not active, the accelerated circulating charge will be sampled prior to the peak value or flattop.

Stop - "Stop Control" halts all operations

*Fermi National Accelerator Laboratory, Batavia, Illinois 60510; operated by Universities Research Association, Inc. under contract with the United States Department of Energy.

0018-9499/79/0600-3448$00.75 © 1979 IEEE

and retains all numeric data displayed.

Start - "Start Control" arms the unit for normal operation on the next cycle of operation. Start control also resets the TPA and stop controls if selected prior to depressing the start control.

Clear - "Clear Control" resets the display readouts to zero, blanks the most significant digit of all display readouts and arms the unit for normal operation on the next machine cycle if the start control is active.

Start/TPA - With the start pre-selected the "Ten Pulse Average Control" arms the TPA mode to begin on the next machine cycle. At that time the most significant digit of all intensity display readouts become active and the charge data will start to accumulate. During the TPA operation all display readouts are updated each machine cycle of operation. The efficiency display readouts are computed and displayed on a per cycle basis. After ten machine cycles have elapsed the unit will automatically select the Stop mode.

In addition to the control push button features there are digit switch modes. Using the digit switch on the right side of the front panel, the user can select a ratio of any of the numbered displays. This feature allows the user to fabricate any combination of interest.

MODE CONTROLS

The digit switch previously discussed in the section heading "Controls" also serves as a mode control sense switch. Special operating options are selectable using predetermined numerical values.

Special mode code #98 selects option 1 and synchronizes the display unit to gather data at a one hertz rate. Option 1 is typically used during accelerator study periods.

Special code #99 selects option 2 and displays data representing a "Figure of Merit". This value is a result of comparing the current Overall efficiency to a value representing the best efficiency attained during previous operation, having the same Average Booster intensity value. Figure of Merit = Present Calculated overall eff./Best Overall eff.

Special code #97 selects option 3 and halts all data acquisition operations. The unit then displays a history of maximum machine performances for the various accelerators. Maximum charge and efficiencies recorded will be displayed to provide the user with a fast reference to past machine performance.

Special code #96 selects option 4 and halts all data acquisition operation, blanks all displays and powers down the unit to a minimum value. This option can be selected when the unit is out of service. Minimum test modes are also available to the user. Special code #88 selects option 5 and halts all data acquisition operations. The unit will then turn on all display segments testing the display for any malfunctions.

Separate from the above options are two more associated with Main Accelerator Storage Mode Studies. When the Main Accelerator is operated in this mode the unit is alerted by a signal from the host computer. Prior to the computer flag, all accumulated data is retained in the display. After the store mode has been entered, elapsed time data, store transition efficiency, percent of charge remaining in the Main Accelerator and the current value of the stored circulating charge are all available to the user by using special codes #94 and #95.

The fore-mentioned unit uses an interrupt driven, subroutine oriented, software control program. Re-entrant subroutines are used to relocate data, perform arithmetic operations and pass parameters to other nested system subroutines.

SYSTEM ARCHITECTURE

The system consists of function modules interconnected by four interface buses. A sixteen bit address bus, an eight bit data bus, an eight bit control bus and an eight bit interrupt bus. The function modules include six kilo-bytes of read-only-memory, seven interface modules, four display modules, one control module, one timing module, three counter modules, one converter module and one central processing unit.

Read Only Memory

These modules contain a resident software program used by the central processing unit to govern system operation. The read only memory also contains data tables needed to establish the alarms and limits feature of the system. This feature is software controlled and can be used to alert the user of abnormal accelerator operation.

Random Access Memory

This module is used for temporary storage of data used in computation, data manipulation and coded data keys used to enable special system functions. The memory is partitioned to perform pre-established system tasks.

Interface Module

These modules are used to interface the special function modules to the micro-computer system. These modules are software programmed and feature two eight bit bidirectional data buses as well as control strobes.

Display Module

These modules are used to distribute numeric data to the front display panel. Using an interface module, data is relocated from read only memory or random access memory to a display module, then stored into the appropriate display readout. All data manipulation is governed exclusively by the resident software program. Each module contains five hard wired buses connecting the display panel readout to a display module. These eight bit buses relocate multiplexed data to the display panel

readout and provide pre-assigned control strobes to each numeric character in the display panel.

Control Module

This module is used to interface the front panel user controls into the micro computer system. Under software control, this module is scanned to determine what mode of operation the user has selected. The module also includes hardware logic circuitry used to reduce the interrogation time of the central processing unit. All user interactions are monitored by this module. High priority user requests interrupt the central processing unit via the eight bit interrupt bus to insure rapid system response. This module also includes software controlled circuitry used for modulating the display readout intensity. Software alarms and limits routines determine if a parameter displayed is out of tolerance and requires its intensity modulation altered to alarm the user.

Timing Module

This module is used to synchronize the unit to accelerator operations. A laboratory distributed clock signal containing time markers provides the means to accomplish this task. Phase reversal techniques are used to set the time markers in the clock signal. The timing module decodes the phase reversals and interrupts the central processing unit to execute appropriate software routines associated with that time reference. Hardware circuitry is used to decode the clock signal leaving the central processing unit free to do higher priority tasks. Output strobes are also generated by this module to synchronize external peripheral system hardware.

Counter Module

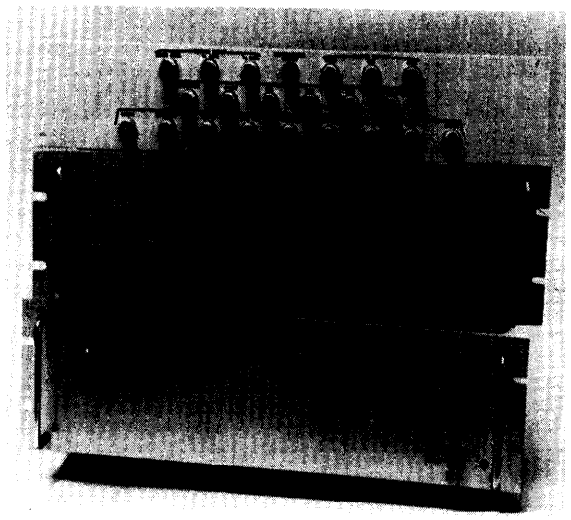
This module stores asynchronously transmitted data pulses from the external peripheral data distribution system. Each five digit binary coded decimal counter output is multiplexed into the micro computer system using hardware circuitry. Under software control each counter digit is interrogated, assigned a digit identification code and stored in random access memory for future data manipulations. Software routines active only at preselected times, insure that the asynchronously transmitted data will be present at the time of execution. The timing module mentioned earlier provides this needed synchronization.

Converter Module

This module outputs preselected data in the form of an analog signal. Under software control, data stored in random access memory is relocated to the convert module binary coded decimal to binary converter. After conversion the software program relocates the new data to the appropriate hardware latch circuitry. The latched ten bit binary data word is then converted into an analog form and outputed to external peripheral system hardware.

Central Processing Unit

This module performs all of the logical tasks dictated by the software program resident in the read only memory modules. It contains all the hardware circuitry needed to support all processor functions. The processor selected is wired to use sixteen address lines, eight bidirectional data lines, eight control lines and two clock input lines. Five of the control lines are used by the system to request special processor modes. Among these are interrupt request, halt, non-maskable interrupt, and reset. The remaining three control lines are used by the processor to request certain system modes of operation. Among these are read, write, valid memory address and data buss available.



Display System

ACKNOWLEDGMENTS

The author wishes to gratefully acknowledge the support and inspiration for this project provided by Dr. F. Turkot. The author also thanks S. Barnhill for her skills and efforts in constructing, debugging and installing the system in a very short period of time. Credit is also due to G. Tool for his concept of using modular design techniques in micro computer applications.

REFERENCES

1. R. K. Richards, "Digital Design", Wiley-Interscience, New York, 1971.

2. John B. Peatmann, "Microcomputer-Based Design", McGraw-Hill, New York, 1977.

3. John D. Lenk, "Handbook of Logic Circuits", Reston, Reston, Va., 1972.

4. Motorola, Inc., "M6800 Micro Processor Programming Manual", Phoenix, Arizona, 1975.

5. Motorola, Inc., "M6800 Micro Processor Applications Manual", Phoenix, Arizona, 1975.