IEEE Transactions on Nuclear Science, Vol. NS-26, No. 3, June 1979

DISTRIBUTED CONTROL SYSTEM FOR THE NATIONAL SYNCHROTRON LIGHT SOURCE.*

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Introduction

The National Synchrotron Light Source[1] at Brookhaven National Laboratory will be a national facility for research groups in a number of experimental fields. The major components of the system are a 2.5 GeV electron storage ring, a 700 MeV electron storage ring, a 700 MeV booster ring and an electron linac of about 100 MeV. The control system will make it possible to control and monitor the accelerator complex from a single control location. Some hundreds of control elements and a similar number of monitored variables must be made accessible to the systems operator in a convenient and effective fashion.

Until recently, accelerator and similar control systems have used modular interface hardware such as CAMAC or DATACON[2] which translated digital computer commands transmitted over some data link into hardware device status and monitoring variables. Such modules possessed little more than local buffering capability in the processing of commands and data. The advent of the micro-processor has made available low cost small computers of significant computational capability. This paper describes how micro-computers including such micro-processors and associated memory, input/output devices and interrupt facilities have been incorporated into a distributed system for the control of the NSLS.

System Objectives

A major objective of the control system is, of course, to provide convenient and effective control of the accelerator complex in its eventual operation. An additional objective is to provide support facilities for the development of accelerator equipment in an environment as similar as possible to that in which it will eventually operate. By developing hardware in the working environment, rather than in various simulation modes it is possible to avoid the major transition and accompanying problems when the equipment is transferred from simulation to operation. To make possible concurrent development of equipment by a number of engineers and physicists in the working environment, time sharing facilities are needed in the control system. These could be provided by a number of development nodes in a computer network or by time-sharing operating systems in one or more individual computers. The scope of the NSLS project and the ultimate needs of the control system have caused us to choose the latter system.

The use of micro-processors within the system has permitted the replacement of control modules by micro-computers which expand the control function both downward to the hardware and upward to the central computer facilities. The first of these expansions allows simplification of the controlling and monitoring devices by using PROM resident "firmware" to perform control functions previously carried out in hard-wired logic. The second expansion permits improved real-time computer response to device needs without a high speed communication system since such response can be provided by the micro-processors without, in general, reference to some larger computer. Further, the algorithms employed in the micro-processor allow devices to be addressed at a higher level, in a logical sense, releasing the central computer facilities from the need to respond and transmit at the elementary operation level. The micro-processor can also be used to translate the detailed requirements of individual devices into a more general form which rationalizes the treatment of data acquisition and control operations within the central computers.

System Configuration

The functional form of the system is shown in figure 1. Two identical control desks in the control room are connected to two Data General ECLIPSE S250 computers with the indicated facilities. These computers are connected to 3 Data General NOVA 3/4 computers via a multicomputer bus called the Multi Computer Adapter (MCA), which allows rapid transfer of data from any computer to any other computer in a system of up to 15 computers. Each Nova is equipped with 16 serial asynchronous full-duplex lines which operate at 38.4 kilo baud. Each of these lines is connected to a micro-computer which is an Intel Multibus‡ compatible system from one of several actual manufacturers. A single board provides all of the basic microcomputer functions together with a serial port and 48 bits of parallel input/output. Additional input/output, a second serial port and a wide variety of interface functions are provided by up to 7 additional boards which can be installed in the Multibus crate.

System Functions

1. Partitioning. In a system with two or more levels of computers, the partitioning of responsibility for system operation provides significant choices. The choices in this system were dictated by the following considerations: a) The central computers are coded in high level language under an advanced operating system which provides generous facilities for development activities; b) The microcomputers are coded in assembly language and operate under minimal systems with few facilities for development. We, therefore, chose to dedicate microcomputers logically and physically to control areas of the accelerators. To minimize the complexity of the microcomputer operation each one performs functions for a single area of the accelerators, such as power supply control for an injection line, control of an RF modulator or interfacing to a set of diagnostic equipment. Sub-division of the system in this way indicates that about 36 microcomputers are needed to control the system. The 48 computer capability thus allows some room for expansion. All other functions of the control system, display generation, acceptance of operator input, data storage and manipulation, record keeping, etc., are performed by the central computers. These functions are performed under the manufacturer's operating system relieving the NSLS staff of the task of providing an operating environment for their execution.

The NOVA computers function solely as message switching and buffering devices to relieve the central computers of responsibility for detailed data transmission activities. The central computers therefore operate on complete incoming or outgoing messages, rather than on bytes or words. The use of NOVA 3/4's for this function was the best solution offered by the manufacturer to the problem of interfacing to a large number of moderate speed asynchronous lines. It has

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‡ Multibus ® Intel Corporation.

0018-9499/79/0600-3387$00.75 © 1979 IEEE

the following properties: a) any central computer can communicate with any micro computer; b) messages to or from the micro computers are buffered and queued within the NOVAS and forwarded to the appropriate recipient; c) the data rate of all lines operating at full speed in both directions cannot be supported but this is statistically unlikely, and overruns are handled in the NOVA software.

The overall configuration adopted has the following advantages:

a) Redundancy. The accelerator system can be operated from a single control desk via either of the ECLIPSE computers. Each NOVA can accept 32 serial lines so that the system can operate with any 2 NOVAS. The system can thus be configured to operate with any computer removed, allowing operation in the presence of hardware failures and disconnection of computers for test or development.

b) Data rates. By partitioning the system as described the 38.4 Kilo Baud data rate is quite adequate for system communications since large blocks of data need never be sent over the communication links. This allows use of inexpensive serial links over long distances;

c) Local monitoring. Symmetrical initiation of messages on the data links allows messages to be generated by the micro-processors. Any micro-processor can monitor the behaviour of equipment and transmit an unsolicited message to the central computer to report errors. This provides the logical equivalent of an interrupt to the central computers in the event of a malfunction or other significant occurrence within the micro-processor controlled sub-system.

d) Reliability. With firmware stored in Read Only Memory (ROM) and appropriate coding, the micro-processor systems are at least as reliable as discrete hardware. In particular, they can be coded to survive or recover from power failures and to continue operation. The central computers are, therefore, coded to operate on the assumption that remote equipment is maintained in a well-defined state by the micro-processor.

e) Expandability. More micro-processors can be added to available or additional serial links. Additional NOVAS or ECLIPSES can be added up to a total of 15 computers if additional computers are needed in the system. These additional computers could communicate with all the micro-processors and all other computers. The generality of the serial, asynchronous transmission scheme adopted, together with the simple software protocol permit the easy substitution of alternative equipment at the remote locations. Should it be desirable in the future to substitute more powerful computers, this can be accomplished with no change in the hardware or software of the remainder of the system.

Choice of Micro Computer

A number of considerations influenced the choice of micro computer used in the system. As noted above, the system does not in itself dictate the choice. Major factors which encouraged the use of a Multibus compatible system were:

a) The Multibus is a completely specified and comprehensive communication bus;

b) Processors and peripheral equipment compatible with the Multibus are available from multiple commercial sources;

c) Bus sharing in a multi-processor environment is permitted by Multibus conventions allowing more powerful systems and further subdivision of the tasks within a single micro-processor system;

d) A high level of integration, such as a complete micro computer on a single board, is provided by many manufacturers.

Software

The ECLIPSES operate under Data General's Advanced Operating System (AOS). This system allows up to 64 independent processes to co-exist within the computer. It provides the terminal handling and file systems necessary for program development and testing and will allow general purpose monitoring system programs to operate in parallel. The NOVA computers will run a dedicated program to handle the message switching function. This program has been specified to Data General whose staff will write the necessary code. The micro-processors have a small resident read-only-memory monitor. This allows a terminal connected to the micro-processor to communicate with a larger computer in a transparent mode which is used for program development. When the code is ready for test it is loaded into the micro-processor and executed with the conventional monitor testing facilities. Standard code exists in the micro-processors to control message receipt and transmission over the serial links and to dispatch on machine-synchronization interrupts. The remainder of the micro-processor code is completely application dependent. Since it is closely coupled to the behaviour of the connected hardware, assembly language coding is appropriate and effective. By restricting the application of the micro-processor to functions requiring fast response and involving detailed correlation between the elements of a specific hardware subsystem, the code can be made simple and manageable in an assembly language environment.

Status of the System

The first ECLIPSE S250 has just been delivered and is undergoing acceptance testing. The NOVA code is being written and will be completed in a few months. Three micro-processor systems have been designed and coded and are being tested with the accelerator hardware. The control desk is being designed and its equipment purchased.

References

1. Blumberg et al., Paper G5 in this conference.
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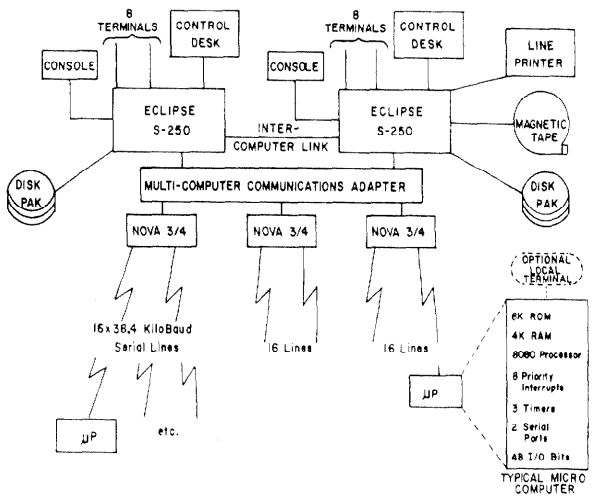

Figure 1. Control System Configuration