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A BROADRANGE BEAM SIGNAL LIMITER FOR THE FERMILAB BOOSTER

E. F. Higgins, Jr.

Fermi National Accelerator Laboratory*
Batavia, Illinois 60510

Introduction

The Fermilab Booster synchrotron is a rapid cycling synchrotron having initial and final energies of 200 MeV and 8 GeV respectively. During acceleration, the frequency of the acceleration voltage tracks the change in proton velocity requiring the rf frequency to tune nearly an octave, from 30-to-53 MHz. The rf tracking signal is derived by a programmable voltage controlled oscillator (VCO), whose frequency is adjusted as close as possible with the aid of a predetermined program. Along with the program, adaptive corrections are applied during the acceleration cycle to force exact correspondence between the developed tracking signal and that which is required by the beam for acceleration. The technique to accomplish this is by phase locking the VCO to a beam-developed control signal obtained from a vacuum line mounted beam detector.

At the beginning of an acceleration cycle, the beam detector voltage is very small, 10-15 mV, P-P, and it is a complex signal, exhibiting a nearly sinusoidal waveform at 30 MHz with a large amount of additive 200 MHz Linac residue. In a few turns, 10μsec or so, however, the bunching processes together with current gain due to increased proton velocity, forms a detector signal having a narrow spike-like doublet form and an increasing magnitude. This process continues, causing the signal to grow until at the end of the cycle it is about 700 mV, P-P, a 35 dB change from its initial value. The raw beam signal is not suitable for direct application to the phase lock circuits without prefiltering and conditioning for amplitude stability.

In practice, a "constant delay" rf limiter/filter is used to stabilize the beam signal and remove objectionable harmonic content prior to application to the phase lock circuits.

This paper will discuss the general problem of beam signal limiting as it applies to the frequency lock loop, give the details of the limiter used, and present specific characteristics of the device used in the Booster synchrotron.

Discussion

The phase-lock circuit used in the Booster is shown simplified in Figure 1. In the figure, the phase detector receives a delayed VCO reference signal together with a beam derived signal from the beam channel. Part of the VCO output is transmitted via a voltage controlled phase shifter to the low-level distribution elements. This phase shifter, driven by the radial position analog and other signals, permits a controllable phase offset from the VCO and allows continuous development of and control of the synchronous phase angle during acceleration. The phase range of the device is $\pm\frac{\pi}{2}$. The phase detector PD, Fig. 1, is implemented by a +7 dBm double balanced mixer. This mixer is arranged so that its dc isolated ports receive the rf information and its IF port (lo-pass port) arranged to develop the phase error signal. A doubly balanced mixer was chosen for this service because of inherent excellent overall stability, broadbandedness, good sensitivity, high isolation, low offset and drift, and amplitude error reduction for mild overdrive above nominal input levels. The mixer configured PD has a transfer function of the form:

$$V(\theta) = K\,AB\,\mathrm{Cos}\Delta\theta + H+N$$

where, $V(\theta)$ = output at IF port
K = gain constant ≈ .5
A,B = input signal amplitude
$\Delta\theta$ = phase difference between inputs
H = harmonic spectrum
N = noise output

Generally the output error $V(\theta)$ is bipolar exhibiting a characteristic "S" shaped value with $\Delta\theta$, and it will be zero valued only for the condition that the inputs are in exact quadrature, i.e., $\mathrm{Cos}\,\frac{\pi}{2} = 0$.

The VCO in Figure 1 is a varactor tuned LC integrated circuit oscillator. The output of the LC circuit is filtered and heavily buffered to minimize loading effects; it is locked to the beam fundamental when the quadrature condition between beam signal and VCO signal is reached. The rf bandpass filter shown in the beam channel aids in removal of beam harmonic content.

System Errors and Limiter Specs

As with any phase detection/conversion process, certain kinds of errors can be developed which are deleterious to the phase locking and holding operation. In the case of the mixer configured PD, the dominant errors are caused by its sensitivity to amplitude modulation of either or both inputs, its sensitivity to the presence of spurious phase errors, i.e., those that are not directly associated with beam dynamics, the presence of a rich harmonic spectrum at the PD output port and the presence of noise transferred via the limiter thru the PD to the VCO.

The reduction or elimination of these error factors requires measures to (1) hard limit the beam signal channel over the 35 dB dynamic range and filter the spectrum to minimize noise effects, (2) prevent spurious phase variations from developing in the beam channel due to large variations in the limiters' signal drive level, (3) remove the harmonic spectrum from the frequency loop active gain devices and thus prevent rectification effects from causing offsets, (4) match the delay paths--VCO signal return path and VCO signal via low level limiter PD path--to prevent frequency related phase differences from developing due to delay differentials and (5) optimize the limiter signal-to-noise ratio SNR to aid in reducing noise sideband components in the VCO output.

Delaying the VCO signal to the PD to match the path thru the acceleration loop is easily accomplished within a few electrical degrees with appropriate cable. The harmonic content of the PD output is easily reduced by > 20 dB with constant impedance lo-pass filtering ahead of the loop gain elements. This

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reduction has been shown to be sufficient to provide negligible offset error. The SNR of the beam signal path is optimized by bandpass filtering and allowing only the minimum forward gain (FG), to be applied in the limiter module; excessive gain although not affecting the signal voltage limit level would reduce the SNR since the non-limited noise level linearly increases with FG. Hard limiting the beam signal without introducing excessive phase shift with input level is a more formidable problem and requires careful limiter selection and design.

The amount of non-beam signal dependent error chargeable to the limiter is a function of several operational parameters such as bending field, required energy gain per turn, the synchronous phase angle required for acceleration, the dynamic range remaining in the variable phase shifter after accounting for all programming during acceleration, and the peak variations in the phase programming. For nominal field excitation, and 80% (765KV/T) of maximum ring voltage, the dynamic range remaining in the phase shifter is nominally 32°. Of this, 75% (24°) must be available for dynamic programming and frequency related errors, while the remaining 25%, (±4°) represents the amount of error allowable for the AM and PM induced phase effects of the limiter. Tests indicated that insertion phase errors were more serious than AM errors for a balanced mixer PD when operating in mild compression. Thus ± 1 deg. of the error budget was assigned to AM error while the remaining ± 3 deg. was assigned to direct insertion phase errors of the limiter. For a mixer configured PD the AM-to-PM transfer error sensitivity is 2 deg./dB change; thus the limiter must have a flatness of ± 0.5 dB in order to meet the ± 1 deg. phase error spec. and no more than ± 3 deg. additional from all other circuit effects.

Limiter Design

Candidate circuits for the limiter design included the "current starved" long tail pair, overdriven amplifier, 2 state IC line receivers, inverters, and comparators, and transformer coupled diode ring quads (mixers). AGC circuits, of course, are often used for amplitude stabilization but the inherent large attack time, variation of phase with the forward amplifier gain, and the high post detector gain needed for good regulation, preclude AGC techniques for critical applications such as in the Booster beam channel.

Investigations of the limiting devices above revealed that the biased transformer coupled quad, mixer, gave the best overall performance, having less than ±1° phase shift with 13 dB range for a single overdriven mixer, in the 30-to-53 MHz range. A cascade of 3 such devices as shown in Figure 2 with appropriate interstage amplifiers and matching networks gave the required 35 dB range with less than ±3° phase shift and better than ±.5 dB flatness as needed. Figure 3 shows the regulation characteristics of the 3 stage device.

The long-tail pair stages were found difficult to match over the large frequency range, exhibited large thruput delays, and required expensive transistors to secure ±5° phase flatness over the 35 dB range at the 53 MHz frequency. The overdriven amplifier device performed best in a narrow bandwidth ≈ 30%, not sufficient for the Booster application,but this technique permits straightforward impedance matching to be achieved. Performance values of < 2 deg over 35 dB were easily obtained with a 4 stage device at 30 MHz. The IC devices, 4-to-6 tandem connected stages, exhibited more than ± 5 deg of phase shift with the required input range, but in general, a 50 dB range with less than ±5° phase variation was easily achieved to about 25 MHz, with each type. AM flatness for the IC limiters was better than 0.3 dB over the 35 dB input range.

For the mixer limiter, a MINICIRCUITS PLS-1 device was chosen as the limiting element. This device has a hard compression range of 13 dB when the diode quad is biased at 2-to-5 ma, see insert Figure 3. The input drive level for these mixers is ≈ 15 dBm. RF amplifiers precede each mixer to establish the input level. The rf amplifiers are constructed with bipolar transistors, type 2N5109, and employ ferrite transformer coupling with frequency selective feedback to adjust the input impedance and secure flat bandwidth. The devices, two kinds with gains of 5 and 26 respectively, have a nominal 50 ohm input and output impedance, bandwidth of 180 MHz and are capable of driving a 50 ohm load to 40 mW minimum.

The amplifiers can be seen in the photograph of Figure 4. Resistive pads are used to secure good rf impedance matching at the mixers' input and output terminals and to aid in establishing the desired mixer drive level. Individual Type 741 operational amplifiers are used in a current source hookup to supply bias currents. A 10-element bandpass filter with -3 dB frequencies of 26 and 59 MHz is used to remove harmonic content at the output of the final limiter stage and an AVANTEK UA152 unit amplifier supplies the required buffering and scaling to the output ports which deliver 0.7 V-P-P to each of two isolated output ports.

The overall design process can be systematized by first establishing the dynamic range, DR, next determining the minimum compression range, MCR, of the mixer and the optimum input drive level, Vm, the minimum forward gain, FG, and lastly determining the SNR at the final limiter stages output port, thus,

1) $DR = 20 \text{ Log } \{\frac{\text{MAX BEAM SIG}}{\text{MIN BEAM SIG}}\}$; dB,

2) MCR = 13 dB, from MIXER data sheets,see Fig. 3 or tests,

3) $N = \frac{DR}{MCR}$, rounded up if mixed number

4) $FG = 20 \text{ Log } \{\frac{Vm_1\ Vm_2\ Vm_3\ V_{out}}{V_{BM}\ V_{01}\ V_{02}\ V_{03}}\}$ + dBΣ matching loss,

where V_m = individual mixers max drive level

V_{out} = design value for limiter putput signal

V_0 = individual mixer output level

V_{BM} = maximum beam input level

and

5) $SNR = 20 \text{ Log } \{\frac{V_{OL}}{\{K(Ta+Te)BeGeZ\}^{\frac{1}{2}}C}\}$

where V_{OL} = last limiter output signal level,

K = Boltzmann's constant; 1.38×10^{-23} Joule/deg Kelvin

T_a = source temperature,

T_e = effective internal noise temperature, °K. of limiter ≈ (F-1) 300°K.

B_e = effective bandwidth to the last limiter stage, Hz.

G_e = effective gain to the last limiter stage, NUMERIC.

Z = terminating impedance, OHMS.
C = constant to convert to peak noise ≈ 4; given worst case condition.

The following table together with Figures 3 and 5 give the overall performance characteristics.

LIMITER PARAMETERS

Characteristic	Value
Type	Double Balanced Mixer
Dynamic Range (DR)	35 dB
Operational Bandwidth	30-53 MHz
Number of Stages (N)	3
Forward Gain (FG)	92 dB
Frequency Range, Filter	26-59 MHz
Input/Output Impedance	50 ohms nominal
AM Variation Over Range	±.25 dB
PM Variation Over Range	±3° max
Insertion Delay	50 ns
SNR	56 dB
Minimum Signal for Limiting	13 mV P-P
Output Level	0.7V-P-P
Packaging	2 wide NIM

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FIGURE 1- BEAM SIGNAL LIMITER IN CONTROL CHANNEL

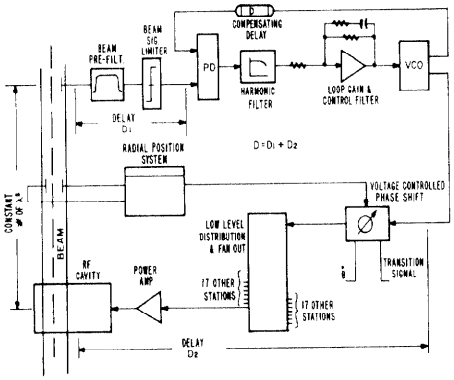


FIGURE 2 - LIMITER FUNCTIONAL DIAGRAM

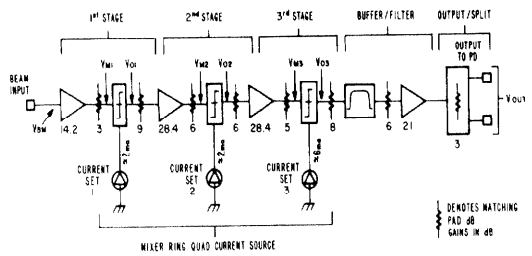
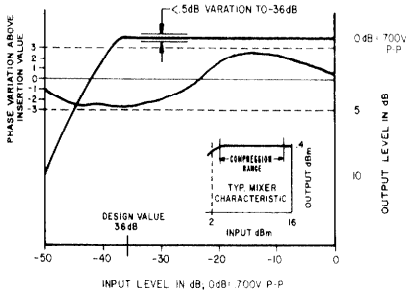


FIGURE 3 – OVERALL LIMITER CHARACTERISTICS



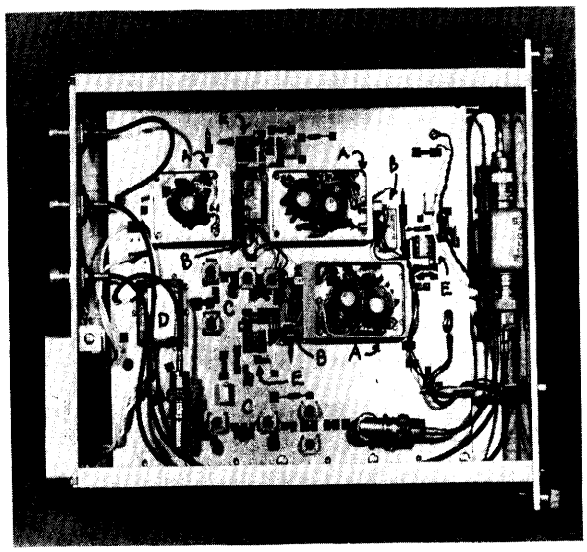


Figure 4. Overall Module View.
A = Interstage rf amplifiers
B = Mixers
C = Bandpass filters
D = Output Buffer Amp
E = Current sources

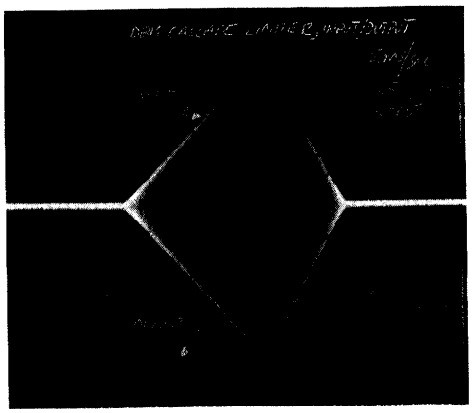


Figure 5. Dynamic Performance.
Note: Output remains constant with large variation in input signal.