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MINICOMPUTER ASSISTED FUNCTION GENERATOR FOR THE DYNAMIC CONTROL OF CHROMATICITY CORRECTION SEXTUPOLES

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Summary

A signal obtained from a function generator is fed to the power supply of the correction sextupole magnets which are used to compensate the chromaticity of the KEK-PS main ring up to flat-top. Main system consists of a minicomputer which generates a set of the digital data forming a function according to the input data. The desired current wave form is approximated by the successive small line segments. The function can be easily changed from the operator console placed in the central control room.

Introduction

When a device is operated dynamically - that is, an input signal to the device is a function of time -, it is required to generate a pulse which is shapable freely to some extent according to the input data. This type of the function generator affords the quick change of the current pattern of the power supply when the new pattern is required.

The magnet system is composed of two serial connection of 16 sextupole magnets. One is connecting 8 magnets placed downstream of the focusing quadrupole magnets and the other is connecting 8 magnets placed downstream of the defocusing quadrupole magnets. Operating both groups independently, it is possible to compensate both horizontal and vertical chromaticity at the same time. Operation of the system can be easily done at the operator console, which is placed 280 m apart from the function generator, through the MODEM. The main part of the function generator is the minicomputer NOVA (model 01) which generates two sets of the digital data from the input data and transfers them to the RAM (random access memory). Then they are converted to the analog function with the digital-to-analog converters (DAC) and fed to the power supplies.

The system is linked with the accelerator control computer (ACC) system[1] MELCOM-70 by the shake hand method to serve to the further study of the accelerator.

Principle of Function Generator

A series of input data is processed step by step to form a function using a core resident program until the "stop" button is pressed. Input data giving a node of the function as shown in Fig.1 consist of two variables - time measured from the trigger (T) and current (I). The CPU (central processing unit) of the minicomputer calculates the gradient of current and its interval immediately after the next input data are obtained and then saves them in the core memory whose data structure is shown in Fig.2.

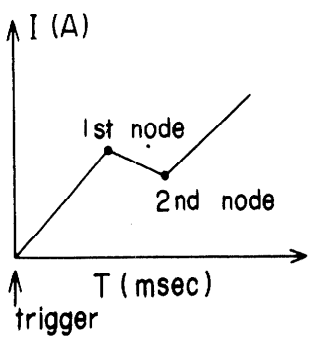
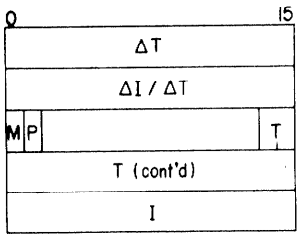


Fig.1
Example of a function



ΔT (time interval, 16 bits), ΔI/ΔT(gradient, 16 bits), T(time, 18 bits), I(current, 16 bits)

M (mode, 1 bit, 0: at rest, 1: operating)

P (polarity, 1 bit, 0: positive, 1: negative)

Fig.2 Data structure of a line segment in the core memory.

A trigger pulse which is coincident with the machine cycle initializes the system and sets the first data (ΔT, ΔI/ΔT, mode and polarity) in latches. Generation of the function for a line segment is made in such a way that the gradient information (ΔI/ΔT) is fed into a reversible counter through the VFC (voltage-to-frequency converter) so as to increase or decrease counts according to the polarity information (P) during the time interval (ΔT). The output of the counter is converted by the DAC (16 bits) to the analog signal which is given to the power supply. Time-up signal obtained from the down counter derives the next data from the RAM and the same operation is repeated until the null data is found. Block diagram for the function generation is given in Fig.3. Gradual change like a staircase is observed in the line segment due to the stairlike change of the up down counter. A series of data is stored in the successive region of the core memory and transferred to the RAM from which data are taken out cyclically to form an analog wave form.

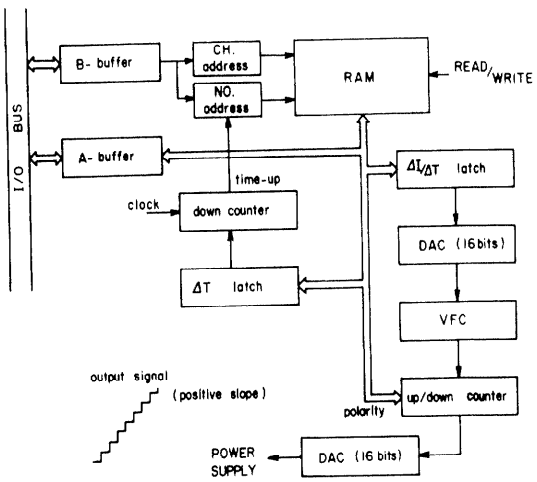


Fig.3 Block diagram of the function generator.

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The system can be divided into two parts. One is what is called the function generator where the analog function is generated from the digital data stored in the RAM without assistance of software whenever the trigger pulse is accepted. The other is the minicomputer which enables to enter the initial data from a keyboard, to convert them into data with the form acceptable to the other part, and to monitor data transferred to the RAM. Transfer of data from the latter to the former can be done by pressing the "transfer" button of the console panel and the transferred data are effective until the system is turned off.

In designing the function generator, the following problems are considered,

(1) Accuracy of conversion from the digital data into the analog function,
(2) Easy operation with the least maintenance.

The conversion to the analog function can be done by using the binary rate multiplier (BRM)[2], the preset counter, or the VFC. Both BRM and preset counter use the clock pulse train from which pulses are selected to be added to or subtracted from counts of the reversible counter. Whereas the VFC uses the constant voltage corresponding to the gradient to make the pulse train to be fed to the reversible counter. The use of the VFC makes the system simple.

Data transfer to the DAC to get the analog function can be made by sending out data from either core memory via CPU or another memory (RAM) independent of the minicomputer. If the important role is imposed on the pure hardware detached from the CPU, troubles associated with operation may be reduced greatly.

Remote Control Station

The main part of the system (Fig.4) is placed near the power supplies in the service house (A41), so the remote control station should be made in the central control room (CCR) to access to minicomputer and to operate the power supplies remotely with the minimal manpower. The remote station has just the same console panel as in the main station. To decide the control place (A41 or CCR) the interlock network is built in.

The transfer rate of the input data to the main control station is 9,600 baud in the form of the 7~2 V negative pulses by a full duplex mode. A numeral is sent serially in 8 bits through the 0.5 mm^2 twist cable. The calculated data ($\Delta I/\Delta T$ and ΔT) are displayed immediately after entering data (T and I). If an irrational data is set, the program detects an error and then flashes the display panel demanding another trial.

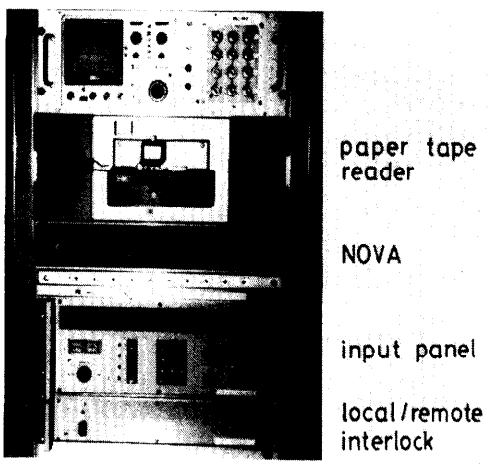

Fig.4 Main control station

I/O Devices

The input and output devices connected to NOVA-CPU are the display panel, the satellite computer of the ACC system and the RAM in the function generator. Each device is accessible by assigning the proper device code in the program. Linkage of these devices are shown in Fig.5 and functions of the data buffers used for the data transfer between NOVA and I/O devices are summerized in Table I.

Input data from the operator console are displayed on the LED (light emitting diode) panel through the BCD (binary coded decimal)-to-decimal decoder. They are stored in the region named data area in the core

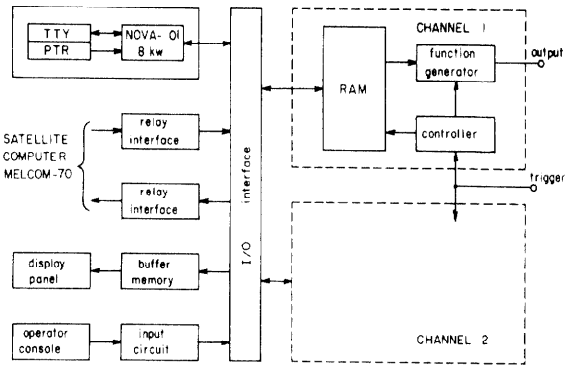

Fig.5 Linkages of I/O devices

Table I Functions of the data buffers

DEVICE	DEVICE CODE	DATA BUFFER
DISPLAY PANEL		① numeral (0~9) ② function key 1 CE 2 CHANNEL 3 NO. 4 T 5 I 6 ENTER 7 STORE 8 END 9 TRANSFER 0 TEN KEY
input	42	A-BUFFER 0 … 15 : ① ② 1:check 0:data set 1:run 0:manual set 1:online 0:offline
output		A-BUFFER (as above)
MELCOM		③ data distinction 1 ΔT 2 $\Delta I/\Delta T$ 3 POLARITY
input	44	A-BUFFER DATA B-BUFFER CH. NO. ③ 1:write(NOVA→MELCOM) 0:read 1:stop 1:start
output		A-BUFFER (as above) B-BUFFER CH. NO. ③ 1:NOVA halt(accidental) 1:online 0:offline
RAM		
input	46	A-BUFFER DATA B BUFFER CH. NO. ③ 1:run 0:rest
output		A-BUFFER (as above) B-BUFFER CH. NO. ③ 1:write(RAM CPU) 0:read 1:run 0:stop

memory and used to calculate ΔT and $\Delta I/\Delta T$ which are also stored in the buffer area for display on the same panel.

For data input and output of the RAM, one must specify the channel address (CH.) and the data number (No.). The channel address selects the channel of the function generator given in Fig.5 and the data number gives the sequential order of the line segments in a channel. More channels up to 31 can be installed in the same fashion.

To link with the ACC system, the I/O interface (Fig.6) to this network is provided. The linkage does not need high speed, so the relay interface is used to communicate by the shake hand method. MELCOM can interrupt into NOVA to read or to write data when the

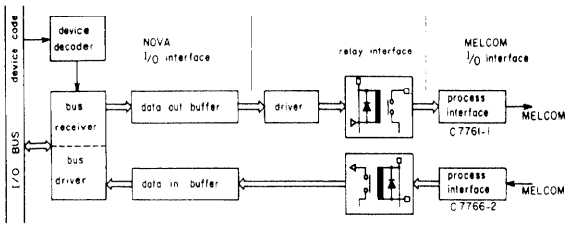

Fig.6 Interface between NOVA and MELCOM

RAM is at the rest time which corresponds to an interval between the end of the function and the next trigger pulse (0.5~1 sec depending on the machine cycle). Start and stop of the function generation can be controlled from MELCOM. When data are sent from MELCOM to NOVA, they are stored in the data area of the core memory and also sent to the RAM according to the channel address and the data number specified by MELCOM. In the reversed case, data specified by MELCOM are sent from the data area of NOVA to MELCOM.

Software

The program using NOVA ASSEMBLY language occupies 3 K words and data the rest of the memory. The program has the following three main roles,

(1) Accept the input data from the operator console,
(2) Accept the command and data from the ACC system,
(3) Generate the function according to the input data, transfer it to the RAM, and compare the function in the RAM with the one saved in the core memory of NOVA.

Input data from the key board shown in Fig.4 are saved in the special region of the core memory named the calculation area for convenience where the successive three data are stored and used to calculate ΔT and $\Delta I/\Delta T$, which are saved with input data (T and I) in the data area. The maximum acceptable data number is 32.

For the check of data in the data area, the "check" button is equipped on the operator console. If this button is pressed, the successive data in the data area can be displayed for the specified channel and data number. Occasionally if one wants to change a part of data, one can change them by giving new data from the key board under the "check" mode.

Data in the RAM are compared with data in the core memory during the rest time at every 10 cycles. If the mismatch is found, data in the core memory are

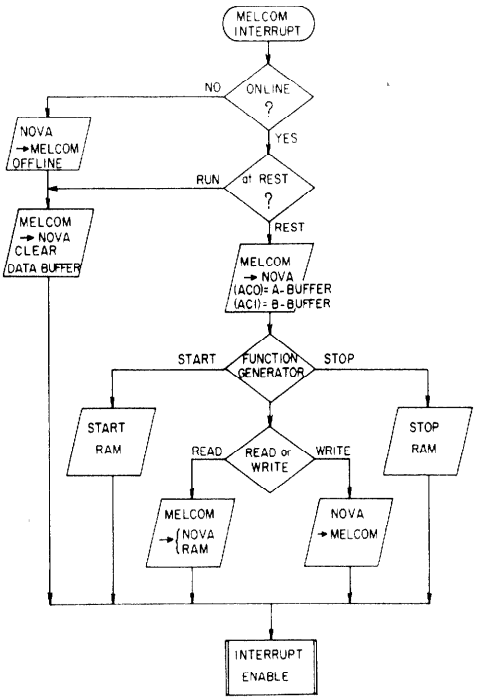

Fig.7 Interrupt from the ACC system

transferred to the RAM. Upper 3 words shown in Fig.2 are stored in the RAM where data are arranged in order.

Communication between NOVA and MELCOM is made as in a flow chart of Fig.7 and the data structures are given in Table 1. Online and offline are selected at the operator console.

Acknowledgment

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References

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