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COMPUTER CONTROL SYSTEM OF MAIN RING MAGNET POWER SUPPLY FOR THE KEK 12 GEV PS

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Summary

The KEK Main Ring Magnet Power Supply is the system for exciting the Magnets, designed for 12 GeV PS. The control system for the power supply utilizes two computers which are interconnected to control and monitor this system. The hardware and software of the computer control system are described.

Introduction

In 1976, a single computer system was introduced;[1,2,3] and it succeeded in accelerating proton beams up to 8 GeV in March, 1976 and 12 GeV in December, 1976. In March, 1978, the control computer system was changed to a dual computer system. The computer system controls three power supplies for bending (B) and quadrupoles (Q_F and Q_D) and succeeded in keeping the magnet current stabilities less than 10^{-3} and 10^{-4} (p-p) for injection and flat top porches respectively. The tracking errors between B and Q magnets were kept better than 3×10^{-3}, in order to accelerate the proton beams effectively. Fig.1 shows the typical current and voltage patterns for 12 GeV operation.

Organization of Power Supply System

The power supply system consists of serially connected multi-stage 12 pulsed SCR rectifiers of Graetz bridge with bypass SCR. The control system for SCR rectifiers is made up of a minor automatic voltage regulator (MAVR) which includes an automatic pulse phase shifter (APPS) to set the firing angle of SCR and a control computer system which supplies the voltage patterns to MAVR. In Fig.2, block diagram surrounded by dotted line shows the computer system. Its function is to perform magnet current regulation by a real time feedback loop, ACR (Automatic Current Regulator).

Control Computer System

Two HIDIC-350's are installed in the control room of the power supply system. The fetch cycle time of the CPU is 0.9 μs. The execution time for addition is 4.5 μs. One (A-CPU) has only a function of controlling. The other (B-CPU) has a function to monitor and execute other background jobs. A block diagram of this system is shown in Fig.3.

Control Computer (A-CPU)

As shown in Fig.3, A-CPU is a core only system and has a memory of 32 kW. The input and output signals of A-CPU are applied to MAVR through a PI/O interface. Data transfers between A and B-CPU are executed through the channel interface (CLC-P). It is necessary for the control computer system that the overhead of the control program must be reduced to minimum, therefore extra peripheral devices are not connected to A-CPU.

CLC-P A and B-CPU are interconnected by a channel interface through CLC-P (Communication Linkage Controller-Parallel), of which the data transfer speed is about 40 kW/ sec.

DCCT Three DCCT's (Direct Current Current Transformer) are used for measuring magnet current. The intrinsic noise on the output signal of the DCCT is attenuated by a low-pass filter so as not to affect current control.

ADC The ADC used to detect magnet current is a very high resolution type, that is, 16 bits unipolar straight binary. Current resolution at the injection porch are 2.7×10^{-4} for bending current and 3.1×10^{-4} for quadrupole current.

DAC The DAC also has very high resolution since a 16 bit bipoler Type is used. ADC and DAC Modules are installed in the temperature controlled cabinet.

Bypass Timing Signals etc. A-CPU sends out the bypass timing signals to the MAVR to change the operation mode of the SCR bridges by a programmed schedule. There are a few signals, which are for interlock and timing purposes between A-CPU and MAVR.

Monitor Computer (B-CPU)

As shown in Fig.3, the main functions of B-CPU are the execution of a program which is called by the input commands entered from operator console. A magnetic drum of which the capacity and access time are 192 kW and 10 ms is used as the main auxiliary memory of a real time operating system, and Cassette M/T is used as off-line auxiliary memory.

Two operator consoles are connected to B-CPU through PI/O interface. One is installed in the local control room of the power supply, the other is in the central control room of accelerator. Either console may be selected by the operators, and has the functions of start and stop of power supply, of injection current monitoring and tracking value fine adjustments, and of displaying the pattern parameters etc.

Software

The operating system for HIDIC-350 is called PMS-II (Process Monitor System - II) which is an on-line real time operating system developed for a general purpose process control system. The source programs available for this system are Assembly Language, Fortran and PCL (Process Control Language).

Program for Control Computer

The control program is resident in the core of A-CPU. This does not work as a task under supervision of PMS-II, but as a task of same priority as PMS-II in order to reduce the overhead of the CPU. So, when this program is running PMS-II does not accept the interrupt signals. The program is composed of 14 subroutines which are executed by schedule of control. The schedule of control is easily changed by the variables in the scheduling subroutine in the control program. The size of the program is about 4 kW.

Control Period The control period of voltage output and feedback current is 10 msec. This period is chosen on the basis of results from a digital simulation of the power supply control system.[4,5,6]

The control schedule is shown in Fig.4. The sub-clock is delayed 5 msec from main clock works so as not to cause time jitter. At present the internal clock of the CPU is used as the control clock, but in the near future this will be changed to an external clock phase-locked to the power line.

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Self Correction (Self Learning) The response characteristics of the power supply control system for the input signal will be very complicated, because the system has higher order transfer functions. So, the calculated patterns might not be suitable for beam acceleration owing to the static errors and transient errors.

To overcome this problem a self learning algorithm has been introduced. By this method operating patterns are corrected using the static errors at each clock pulse. The voltage patterns are corrected by the following equation.

$$\overline{V(t_n)} = V(t_n) + \sum_j K_j \overline{\Delta I(t_{n+j})}$$

where

- V: Calculated voltage pattern (V)
- $\overline{V}$: Corrected voltage pattern (V)
- ΔI: Static error of current control (A)
- j: Time index (j=0,1,2,...)
- K_j: Gain of self learning control (V/A)
- t_n: n-th clock.

The self learning control program is not always running, but may start by a command entered from operator console. The reason is that small errors can only be corrected by ACR feedback and load magnet current does not change with time under routine operation. Only by several cycles of self correction may the operating pattern suitable for beam acceleration be made.

Other Control Signals A-CPU sends out according to the clock schedule, bypass timing signals, timing pulses, current data for the tracking error monitor and reference voltage patterns to the dynamic filter which detects voltage ripples.

Program for Monitor Computer

B-CPU executes many core resident and core non-resident tasks with real time or background under the supervision of PMS-II. About 120 kW of system and application programs, and 70 kW of pattern data files occupy the DRUM memory. Almost all of the source statements for application programs are written by PCL.

Operating Pattern Generation Program The operating patterns are calculated based on B magnet current pattern which takes into consideration saturation of magnet field and inductance, magnet coil resistances, dead time of control system, and a field tracking between B and Q magnets. Fig.5 shows the procedure for pattern generation. The calculated patterns will be stored in the pattern files of the DRUM by the operator's input command. The size of a pattern is about 3.6 kW.

Program for Pattern Supervision This program has various functions, that is, entry and deletion of patterns, making up the tables of pattern parameters and output of pattern data etc.. It may be executed at the time when the starting commands are entered from T/W or operator console panel, whether the power supply is running or not.

Program Supporting Operator Console The information entered in B-CPU from the operator console is transmitted to A-CPU through CLC-P.

Run and Stop Process The operation of each B,Q_F and Q_D magnet power supply can be started independently. Selection of operating patterns is performed by three decimal digital switches. B-CPU reads out the operating pattern from DRUM and transfers it to A-CPU and then sends a starting command to A-CPU.

Fine Adjustment of Injection Current This function has been prepared for making fine tuning of injection energy to compensate for the energy change of proton beams from Booster Ring. The range of fine adjustment is ±5 %.

Fine Adjustment of Tracking Value In slow beam extraction the tracking value must be shifted to the point on the flat top corresponding to the different extraction modes. The Q magnet current pattern data at every control clock can be adjusted by the operator. The magnitude and time of fine adjustment can be entered in B-CPU by digital switches on the operator console. The range of fine adjustment is ±4 %.

Data Transfer

The data transfer between A and B-CPU takes place at every 10 msec control clock time through CLC-P. This method makes for a large overhead in A-CPU, but this is not a problem because of the small amount of data are transferred at one time. The merit of this method is that the development of software will be simple because the system commands to be transfered need not be buffered in the core table. The program for the data transfer is directly combined with the control program and runs after the control program as shown in Fig.4.

Discussion

A typical example of measurements of ACR errors at 12 GeV operation are shown in Fig.6. It is found that there are conspicuous difference between the data for before and after self correction. But there remain small ACR error signals at the point of rapid change of operating patterns. The problem of a computer control system is that it is essentially a sampling system, so the control period has direct relation to current stability. Moreover the power supply has a peculiarity in that the firing of the SCR gate is also a sampling system. Some of these problems are discussed in the following.

Control Clock

The internal clock of CPU has been used as the control clock, but this causes jitters of the time interval between the bypass timing control signal and real firing time of the bypass SCR. For this reason, there arise random components in the ACR error signals and it may be difficult to reduce these random components by pattern correction. Consequently it would be better to use a clock pulse phase-locked with the power line. This will be done in the near future. The control performance would also be improved by shortening the clock interval.

Pattern Generation

A few problems remain in the pattern generation method. At present, the computer cannot correct the relation functions between magnet current, field and inductance. Therefore it has been difficult to obtain optimum relations between these parameters.

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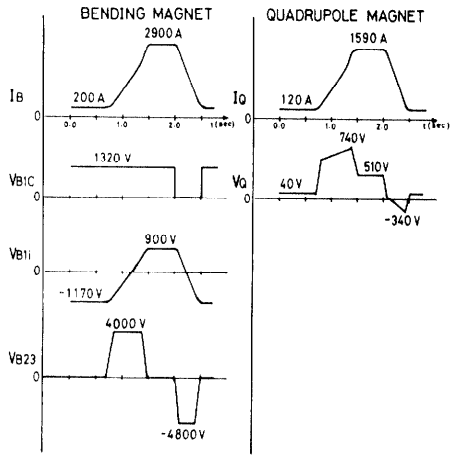

Fig.1 Typical Patterns of 12 GeV Operation.

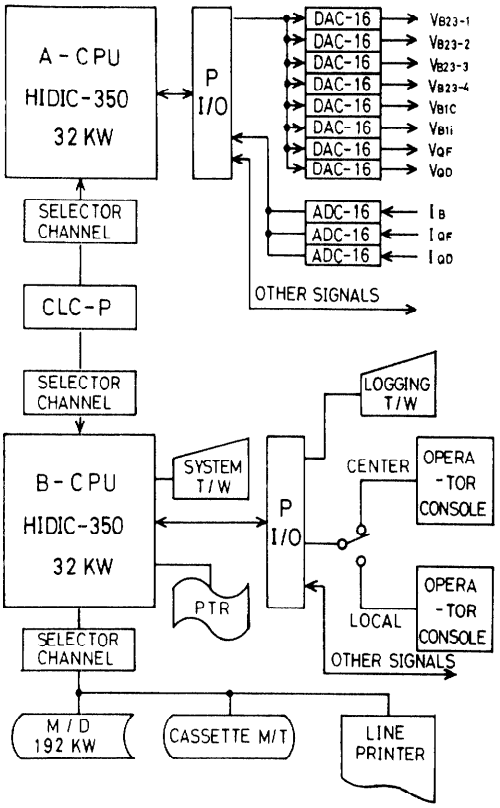

Fig.3 Block Diagram of Computer System.

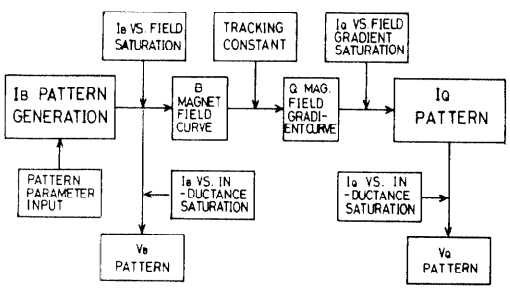

Fig.5 Pattern Generation Procedure.

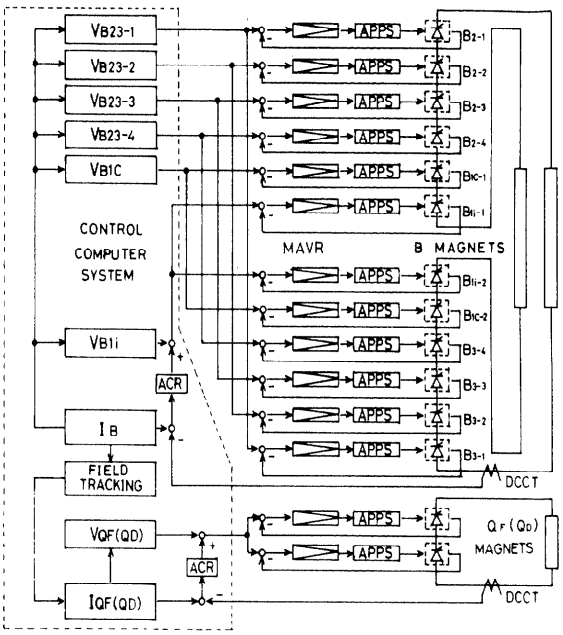

Fig.2 Block Diagram of Power Supply Control System.

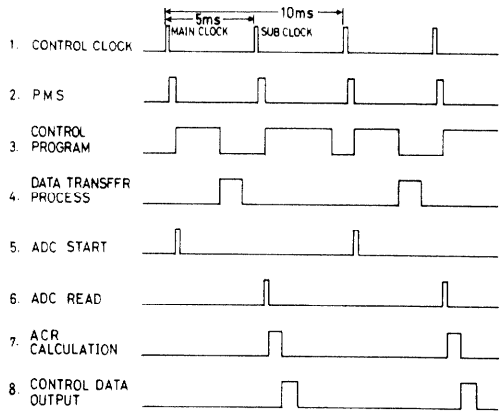

Fig.4 Control Program Schedule.

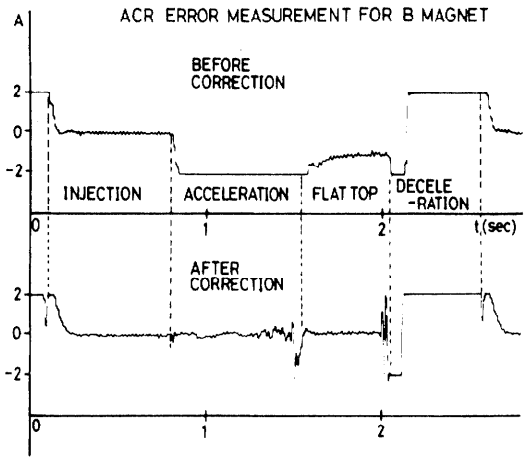

Fig.6 ACR Errors for 12 GeV Operation