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A FAST DIGITIZER AND DISPLAY SYSTEM

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INTRODUCTION

Turn-by-turn information about beam characteristics in an accelerator is a valuable diagnostic aid to accelerator study and development. This is especially true at moments of trauma in an accelerator's cycle such as injection, transition, the instant at which beam is inexplicably lost, etc. The ability to measure several parameters simultaneously on each turn for a hundred or more turns and then display the parameters for viewing, analysis and possible correlation can be a useful aid in troubleshooting, tuning or conducting experiments to study the accelerator.

A fast Digitizer and Display System has been built which takes up to four simultaneous "snapshots" of beam or related parameters during 256 consecutive passes at one or more detection points in the accelerator. The four digitizers may be separated by hundreds of feet so they can be located near the signal source. Each digitizer is connected to a central receiver unit by a single coaxial cable, so distance is limited only by attenuation in this cable. The digitizer output for each measurement is stored in a 256 word memory at the receiver location. The contents of up to four memories provide the input to a multiplexed D/A converter to reconstruct the original analog signals for continuous viewing on an oscilloscope until the information is updated during the next accelerator cycle. The stored information is also available for computer input.

The system is used for Fermilab Main Accelerator development and injection tuning in which the measurement period is 21μsec. It is capable of digitizing every 1.5μsec for use on sequential turns of the Fermilab Booster Accelerator.

GENERAL DESCRIPTION

The Digitizer and Display System is made up of 1 to 4 Digitizer-Transmitters, the same number of Receiver-Memories, a Display Generator, a small Control Panel, and an ordinary oscilloscope as shown in Fig. 1, a block diagram of the system. The Digitizer-Transmitters can be located separately, or up to three channels including their power supply can be housed together in one chassis. The four Receiver-Memories are housed together with the Display Generator circuitry in a chassis which is externally-powered and connected to the Control Panel via a multiconductor cable. Fig. 2 is a photograph showing the receiver chassis with 3 channels installed, a 3-channel transmitter chassis, and the Control Panel. Most parts of the system are constructed as modules using 5.25 in high NIM hardware. A printed-circuit card edge connector is used to interface the module to the bin rather than the 42 contact NIM module connector for ease in bussing power, ground, and signals in the bin. The module connector is then part of the p.c. card layout, rather than an extra item to be assembled. The Control Panel provides a means of changing the display characteristics and controlling intensified markers on the display which identify selected measurements.

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DIGITIZER-TRANSMITTER

Acquisition of the data at the signal source and transmission of the data to the receiver is performed by a Digitizer-Transmitter. It is composed of three modules, designated DCL, ADC, and XMT. When powered and interconnected, these three modules serve as a "sampling head" for one of the channels in the system. A simplified block diagram of a Digitizer-Transmitter is shown in Fig. 3.

The signal to be digitized is applied to the ANALOG IN connector and a trigger for each desired sample is applied to the DIGITIZE input. The digitizer will only respond to these triggers if it has been armed by a pulse on the ARM input. The ARM feature allows one to choose the exact start of digitizing without concern for triggers arriving outside the time of interest. Once armed, the digitizer responds to the next 256 DIGITIZE triggers and then stops until the next ARM. This number of events corresponds of course to exactly the length of memory available for storage at the receiver. If this string of samples is interrupted by lack of triggers before the 256 events have occurred, substitute triggers are generated and enough zero words are sent to the Receiver to fill out the 256 words of memory. This assures that information from two separate time periods will not be displayed as parts of the same waveform.

The digitized sample exits from the 10-bit, 1μsec A/D Converter as a parallel word. These 10 bits plus 2 message header bits plus a parity bit generated from the data are combined into a 13-bit word and converted into a serial pulse train whose format is indicated in Fig. 1. This serial word is encoded in bi-polar Di-Phase code, allowing convenient transformer coupling at the output of a line driver to reduce noise that could be caused by transmitter-receiver ground potential differences.[1] A 15 MHz bit rate was chosen for transmission and digitizing and transmitting are overlapped to achieve a minimum period of 1.5μsec.

RECEIVER-MEMORY

The serial bi-polar pulse train originating at the transmitter is carried by a 50 ohm coaxial cable to the receiver where it is transformer-coupled to a termination resistor and the receiver input circuit. The quality of cable required depends upon the distance. The 15 MHz bit rate (30 MHz components) and simple receiving circuitry allow use of RG-58 for only a few hundred feet. RG-213 is usable for distances approaching 2000 ft. Repeaters may of course be used in the transmission line to allow arbitrarily long distances.

A block diagram of the Receiver-Memory unit is shown in Fig. 4. It is composed of two modules, designated RMC and MEM. The Receiver converts the bi-polar signal to a uni-polar Di-Phase coded pulse train which is decoded and fed to a serial-to-parallel converter. As the first bit, which is always a 1, exits from the converter, it starts the timing sequence necessary to write the 10-bit data word into memory, increment the memory address counter, and clear the serial channel to await the next transmission. The presence of a 1 in the second bit signifies the first word of the 256 word string, causing the memory address counter to be cleared to 0 before writing.

The last 11 bits are checked for parity, and if correct, the 10-bit data word is written into memory. If parity is incorrect, a zero is stored in place of the suspect data. The error checking used in the system is very rudimentary, but the action of simply replacing a suspect quantity by zero is adequate for a signal containing many points to be used primarily for viewing. Since the next word to be transmitted may be directly behind the one just received, there is insufficient time to cause a re-transmission. If maintaining data integrity were a paramount consideration, then all 256 words would have to be stored at the transmitter as well as at the receiver, and more sophisticated two-way transmission would occur when the transmitter memory was filled.

The memory is composed of 10 256-bit bi-polar random-access memory integrated circuits. As one can see from Fig. 4, the memory module contains its own address counter which is simply cleared and incremented by the receiver as determined by the arrival of information at the receiver. However, when the memory is accessed by the Display Generator, a full address word is passed to the counter for loading. The conflict between these two actions is resolved by the receiver having priority, locking out the Display Generator via the WR line. This lockout is continuous during the time all 256 words are being received. If transmission is interrupted, a time-out returns control to the Display Generator.

DISPLAY GENERATOR AND CONTROL PANEL

The information which has been stored in one to four memory modules corresponds to a series of measurements made during a specific time segment of the accelerator cycle. This information is presented to a viewer until the next update time by the Display Generator circuitry which is partially housed in MPX, MDD, and LD modules of the receiver chassis and partially in the Control Panel. A block diagram of this portion of the system is shown in Fig. 5.

The Control Panel provides the viewer with a means of changing the display characteristics and of identifying the "event number" of points of interest in the display. Any combination of the four channels may be chosen for the display, and the relative gain and position of the channels on the display may be varied. The Control Panel counts events as they are displayed and creates two intensity-modulated markers on the display for events which are selected by knobs on the panel. A numeric display on the panel reads out the event number of the first marker or the number of events from the first marker to the second.

An internal 128 kHz clock and 0-255 counter cycle the Display Generator through all of the words in a memory. At the end of one memory's read sequence, the channel select circuitry switches the multiplexer to the memory of the next active channel, and selects the proper gain and dc offset for that channel's portion of the display. A dead time is inserted between the different channel segments to allow retriggering of the display oscilloscope and to allow easy recognition of the beginning of a trace.

The timing and intensity modulation circuitry produce a distinct baseline for each of the displayed channels to help in evaluation of the displayed information. A photograph of a typical 2-channel display is shown in Fig. 6.

If a viewer sees a particular display which he wishes to photograph or study in detail, he may switch to a HOLD mode in which the present contents of all memories is maintained for continuous viewing until the UPDATE mode is again selected. A typical use of this feature is to hold a vertical or horizontal position signal while one moves the markers to separated peaks of oscillation and notes the number of turns between peaks on the numeric display.

ACKNOWLEDGMENTS

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REFERENCES

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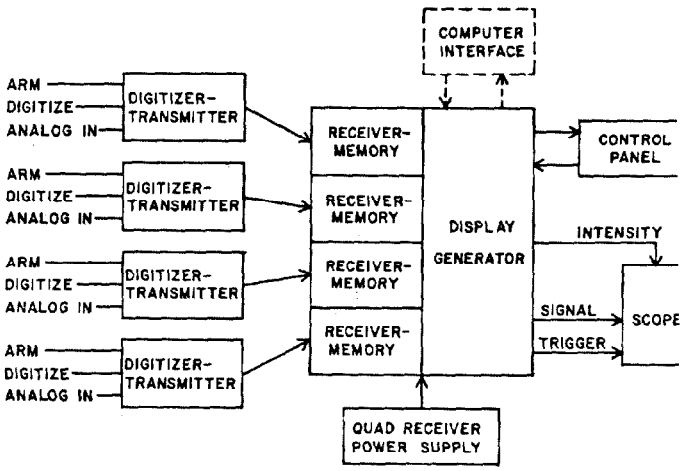

Fig. 1. Digitizer-Display System Block Diagram.

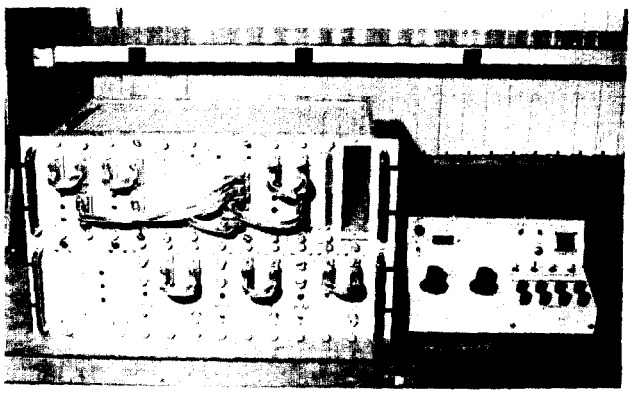

Fig. 2. Receiver Chassis with 3-Channels Installed, 3-Channel Transmitter Chassis, and Control Panel.

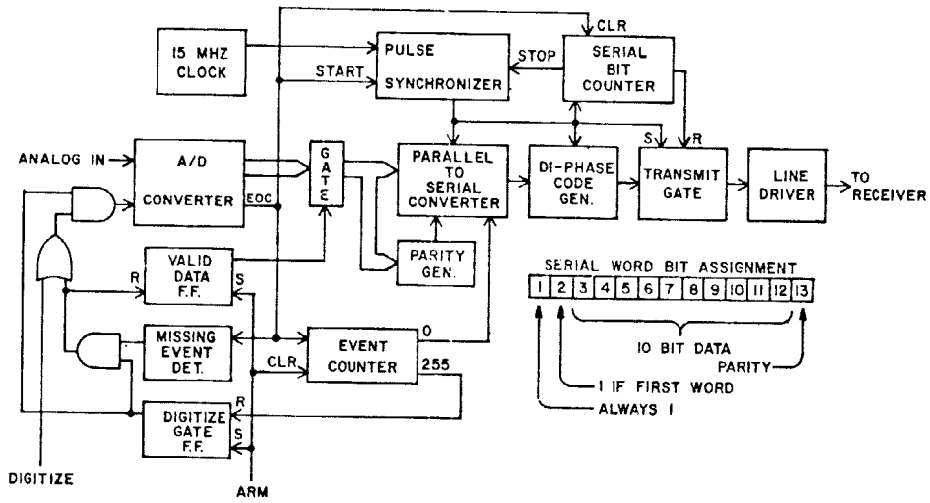

Fig. 3. Digitizer-Transmitter Block Diagram.

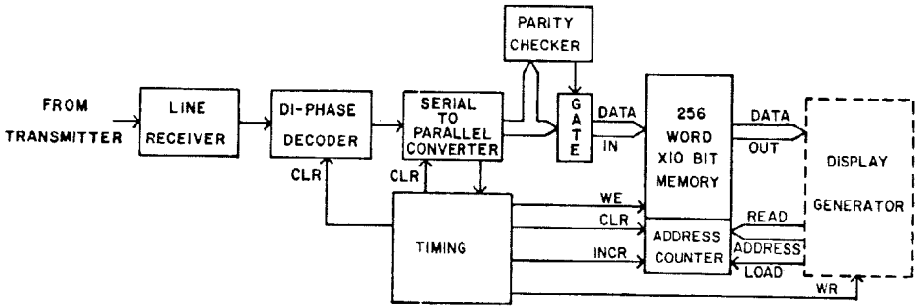

Fig. 4. Receiver-Memory Block Diagram.

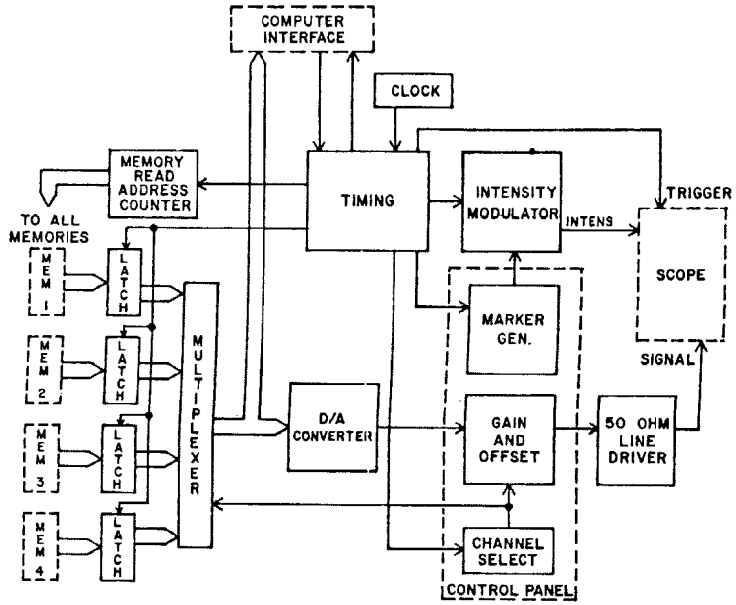

Fig. 5. Display Generator and Control Panel Block Diagram.

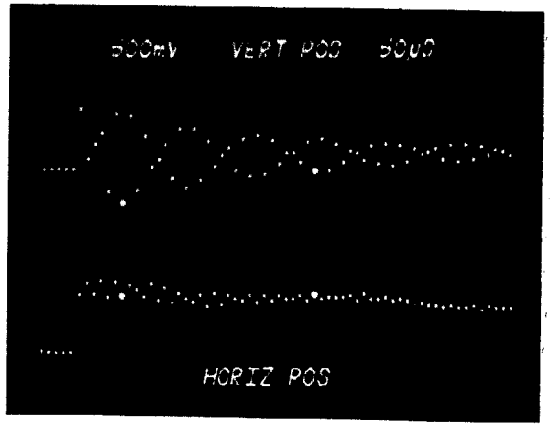

Fig. 6. Typical 2-Channel Display of Main Accelerator Beam Position at Injection. Markers can be seen on Events 7 and 34.