IEEE Transactions on Nuclear Science, Vol.NS-22, No.3, 1975

A VARIABLE-LENGTH TIME DELAY FOR 50 MHz SAMPLED ANALOG SIGNALS

R. Biwer and G. Tool
Fermi National Accelerator Laboratory*
P. O. Box 500
Batavia, Illinois 60510

INTRODUCTION

A Super Beam Damper which makes independent corrections to each of the 1113 beam bunches in the Fermilab Main Accelerator has been built to damp vertical instabilities at high intensity. As the 53 MHz beam bunches pass a point in the accelerator, a position measurement made for each bunch is delayed for one turn around the accelerator (21μsec) and is then applied to a correction device when that bunch arrives. This process occurs continuously for each bunch. This paper describes the 1-turn signal delay hardware.

Signal Delay System Description

The three major components of the delay system, an A/D converter, a Digital Delay unit, and a D/A converter are shown in Fig. 1, a block diagram of the Super Beam Damper. Fig. 2 is a photograph of the delay system installed in the accelerator. The system is capable of operating at clock rates of 26 MHz to 65 MHz and provides a delay of 256 to 1280 clock periods for analog signals in the range of ± 2.5 volts.

The incoming analog signal is sampled and digitized at the 53 MHz RF clock rate. The result, a 5-bit digital word, is then entered into the Digital Delay unit which acts as a variable length, 5-bit wide shift register for the digital word. After a preselected number of clock cycles, the 5-bit word exits from the delay unit to the D/A converters where it is restored to its original analog level. A new sample is digitized every clock pulse while another digital word is restored to an analog voltage thus causing the input analog signal to be reconstructed a precise number of clock pulses after it arrived at the input to the system. A simplified timing diagram relating the input and output signals is shown on the block diagram. Only a segment of the input and output waveforms lasting for a few RF cycles is shown for clarity.

This process could serve as a delay for any analog signal within the limitations imposed by the sampling rate and the resolution of the 5-bit digital word. If the analog signal is random with respect to the sampling rate, the system is not useful for analog signal frequencies above 1/2 f_{clock}. However, if the analog input signal is a sequence of steps occuring at the clock frequency such that digitizing may occur synchronously with the changing steps, then the input waveform reproduction is limited only by the rise time and resolution of the converters.

A number of features are included in the system to aid accelerator experiments. These features include capabilities to:

1. provide normal correction to every other bunch while providing (a) no correction to alternate bunches, or (b) inverted correction to alternate bunches;

2. externally gate the output of the digital delay such that only particular bunches in the accelerator are affected;

3. externally gate an inverted correction to selected bunches in order to reinforce their vertical oscillations, knocking them out of the accelerator to create precise notches in the circulating beam. This latter feature is used for creating notches at injection when beam energy is lowest for the benefit of energy doubler extraction kicker studies.

All operational controls of the delay system such as delay value, special feature selection, and external gate enabling are remotely controlled and monitored via the Accelerator Control System.

A/D Converter

The A/D Converter is a commercially available ± 2.5 volt input range unit capable of digitizing at a 55 MHz rate. The parallel 5-bit binary output is at ECL levels. The input signal routing and input amplifier were rebuilt to provide adequate bandwidth to allow digitizing of the 19 ns period step input shown in Fig. 1. Although the unit is capable of a 55 MHz throughput rate (18 ns period), the insertion delay is 37 ns. As delivered, the timing did not properly resolve this conflict between repetition rate and insertion delay, resulting in multiple output codes whenever the input analog signal was at a code transition level. Replacement of a one-shot delay with a passive delay line and revision of the analog input have resulted in a unit which now successfully digitizes a 65 MHz rate step input.

Digital Delay Unit

The Digital Delay provides the precise variable delay for the 5-bit digital equivalent of the original analog input sampled by the A/D converter. Externally, the unit functions as a 6-bit wide (an extra bit to allow for a future higher-resolution A/D converter) shift register with a variable length of 256 to 1280 bits. The throughput delay for the digital word is the preselected number of clock cycles plus 64 ns insertion delay. Internally, the shift register is constructed of ECL random-access memory integrated circuits forming a sequentially-addressed memory stack into which one is writing a word and from which one is reading a word simultaneously on every clock cycle. This architecture significantly reduces the cost and number of components. Schematically one can think of this memory as a cylinder, shown in Fig. 3, with separate write and read addresses revolving around the cylinder at the clock rate, separated from each other by the desired number of delay cycles. Since there is not a one-to-one relationship among memory length, number of beam bunches, and number of delay cycles, information for a given beam bunch is not kept in a dedicated location.

A memory I.C. can either be written or read at any given time, but cannot be activated in both modes at once. Therefore, the cylinder must be segmented into blocks which are at least as long as the number of words in an I.C. package and protection must be provided to insure that writing and reading cannot occur simultaneously in a block. Our memory is 1536 words long, segmented into six groups of 256 words each. This partitioning determines the delay range of 256-1280 cycles. Each memory I.C. has 128 1-bit words, but since the fastest units available would not allow direct operation at a 53 MHz rate, we actually have two "half-memories" which are addressed together at

*Operated by Universities Research Association, Inc. Under Contract with the United States Energy Research and Development Administration.

one-half the input clock rate, making the effective block length 256 words. As indicated in the Digital Delay Unit Block Diagram, Fig. 4, input words are alternately stored into and retrieved from the "left" and "right" half-memories. Each half-memory thus has 2 clock cycles (38 ns) to be written or read, but the addressing of the two halves is shifted in time by one RF clock cycle in order to achieve the 19 ns clock rate.

All circuitry used in the dynamic operations on the data is implemented with ECL-10000 series I.C.'s. All timing adjustments are accomplished by selecting taps on passive delay lines. Static circuitry involved with front panel or Accelerator Control System input/output is implemented with TTL logic due to its greater availability of complex function circuits.

A photograph of the chassis, Fig. 5, shows additional construction details. Ribbon cable, terminated in its characteristic impedance of 100 ohms, is used throughout for data bussing. All logic circuitry is housed on 4 swing-out wire-wrap planes having individual plug-in sockets for each I.C. pin. Three-layer boards provide interconnection planes for ground, V_{cc} and V_{tt} in the ECL circuitry. Low impedance power bussing interconnects the planes. The receiving ends of all wire-wrap signal lines are parallel-terminated in their characteristic impedance using internally bypassed DIP termination networks.

D/A Converter

The power amplifiers which drive the Beam Damper electrodes require two drive signals which are 180° out of phase. The digital output of the delay unit is used to form a normal and inverted pair of digital words which drive a pair of identical D/A converters. The D/A output must drive the power amplifier 50 ohm input to + 2.5 volts with rise and fall times that are not significant fractions of the total 19 ns period. Commercial units satisfying these specifications are not available. A simplified schematic of the D/A converter circuit is shown in Fig. 6. The + 2.5 volt range analog output is developed by switching on weighted constant-current sources into a 50 ohm output load resistor which is the termination for the cable transporting the signal to the power amplifier. The unit was constructed with 6-bit capability although 5-bits are presently used. The 3 ns rise-time current switches are implemented using DMOS dual-gate FET's driven by ECL-TTL converter I.C.'s. The rise-time limit is imposed by capacitance at the output node. The total converter rise time is maintained at 5 ns by using a circular printed circuit card layout in which all current sources feed to the center where they are collected by a coaxial cable which takes the summed currents to the matched-impedance load. This construction technique provides a minimum capacitance configuration. Due to the closed-loop nature of the Beam Damper application, linearity and dc offset drift parameters are not critical, allowing rise-time to be optimized.

Acknowledgments

The authors wish to gratefully acknowledge the support and inspiration for this project provided by Dr. R. Stiening. We thank S. Barnhill, A. Fogle, R. Hively, and J. Ziober for their skills and efforts in constructing, debugging and installing the system in a very short period of time.

References

1. E. Higgins, Q. Kerns, H. Miller, B. Prichard, R. Stiening, G. Tool, The Fermilab Transverse Instability Active Damping System paper I-3, this conference.

2. E. F. Higgins, Beam Signal Processing for the Fermilab Longitudinal and Transverse Beam Damping Systems, paper I-19, this conference.

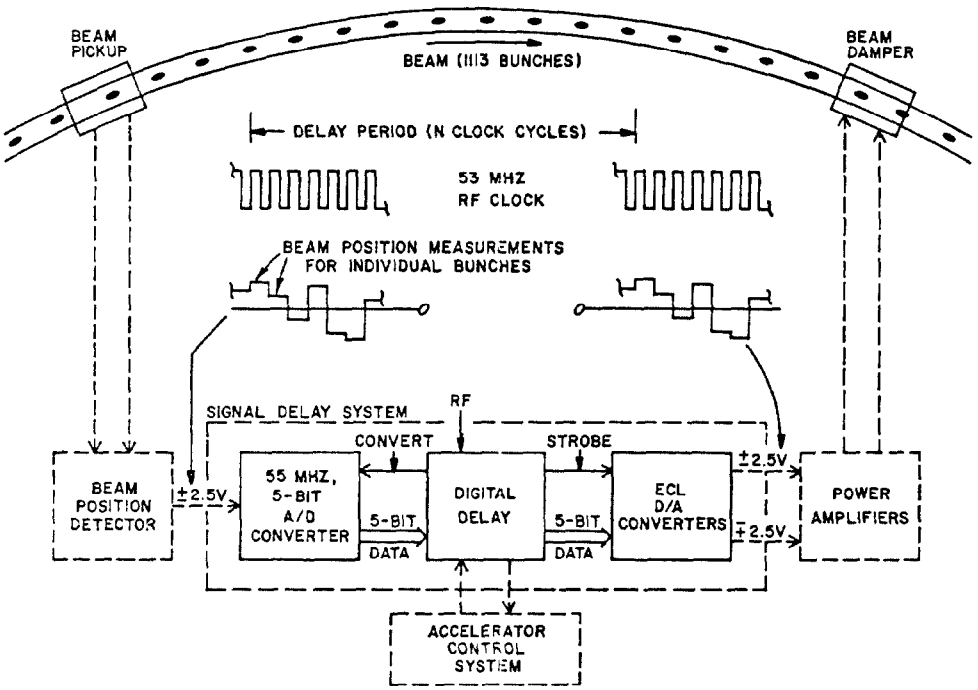

Fig. 1. Super Beam Damper Block Diagram.

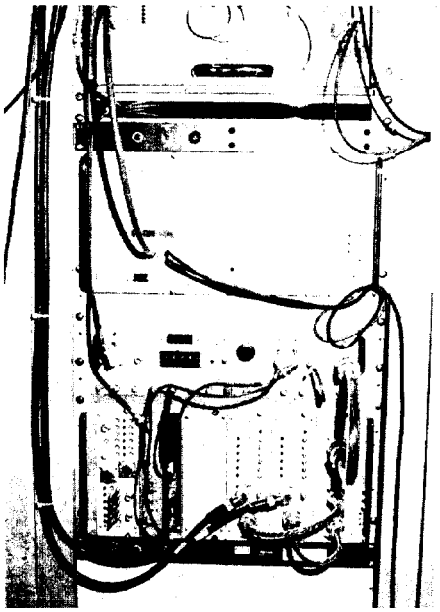

Fig. 2. Signal Delay System.

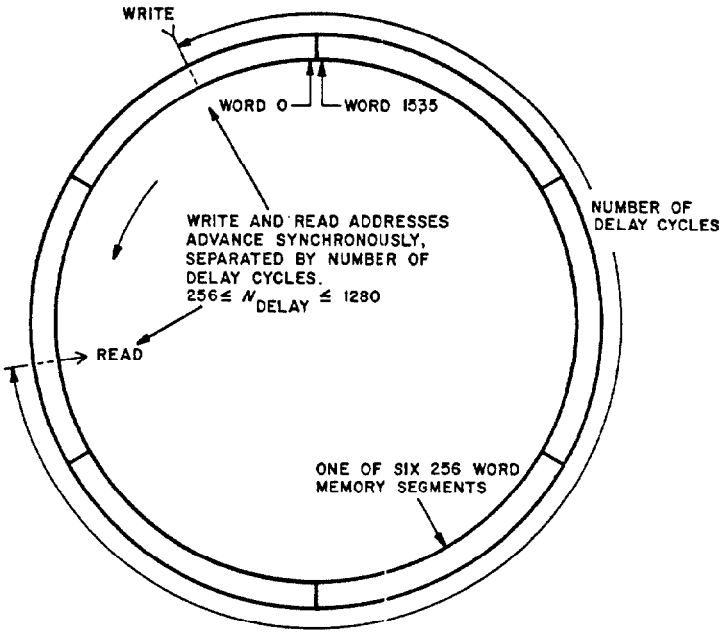

Fig. 3. Cylindrical Memory Model.

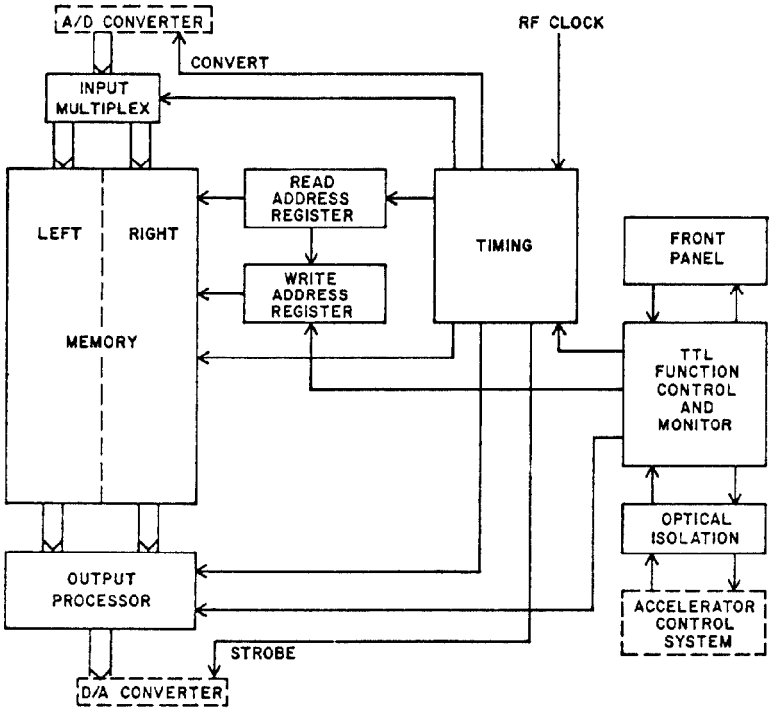

Fig. 4. Digital Delay Unit Block Diagram.

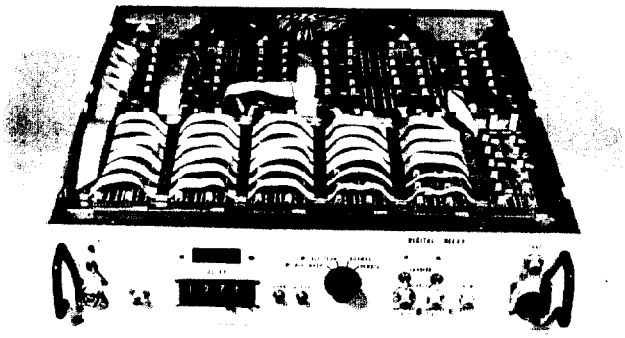

Fig. 5. Digital Delay Unit.

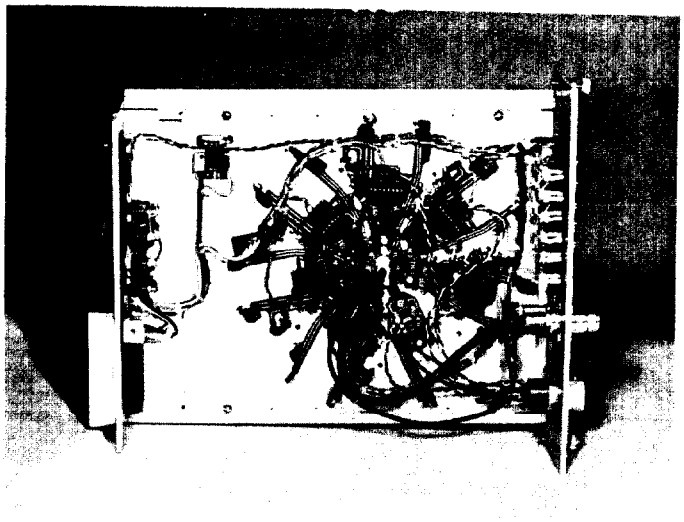

Fig. 7. D/A Converter Module.

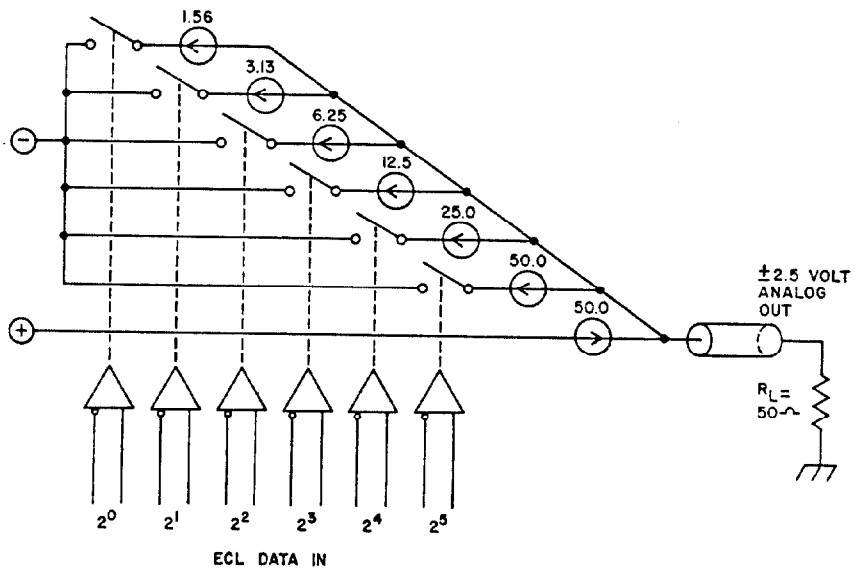

Fig. 6. Simplified D/A Converter Schematic.