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APPLICATIONS OF MICROPROCESSORS IN ACCELERATORS

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Summary

Microprocessors (μP) are finding a growing list of applications in accelerators and associated equipment. μP's may be used as autonomous data loggers and process controllers and in distributed systems.

A μP is essentially a computer CPU. Applying μP, centers around two distinct problems - completing the μP into a computer and interfacing the computer to its environment. The computer can be completed with standard computer components. CAMAC was chosen to be the interface to the environment. CAMAC has several advantages at Fermilab. It is widely used, special function modules for accelerators have already been developed, and many accelerator personnel are familiar with it. Also, it is becoming more widely accepted internationally. A brief description of the CAMAC system is given.

Components and Interfaces

Microprocessor and Systems Components

Typically, a μP contains an accumulator, several scratch pad registers, a program counter, logic for vectored interrupts, instruction decoder, and buffers for interfacing to external components. The μP architecture is fixed, but the designer has full freedom in structuring the memory, I/O and interrupts as required.

If the designer decides to have interrupts, there are many choices. All the interrupts may be "OR'ed" for one master interrupt. Multiple priorities may be fixed or programmable. Each interrupt level may be separately enabled or disabled.

The manufacturers of μP's provide sophisticated integrated circuits (IC) for I/O interfaces. These IC's will synchronize asychronous data, transmit and receive bit or byte serial data and generate clocking, stop-start bits and interrupts for received data.

Memory requirements are determined by the program size and amount of data to be collected and held at one time. Typically, program instructions are burned into programmable read only memories (PROM). The program becomes part of the physical make up of the PROM and cannot be altered by the μP or loss of power. The μP, using PROM's, is ready to start the program as soon as power is applied. This is necessary if the μP is imbedded in other equipment or is not provided with peripherals. Some PROM's can be erased by ultraviolet light and reused.

Random access memory (RAM) is memory that μP's can modify. RAM is used for temporary storage of data and program variables. Nearly all RAM's provided for μP's are semiconductors, which lose stored information if powered down. In addition, μP's may be halted by external strobes, allowing external devices, such as block storage devices, direct memory access (DMA).

Instruction sets of the μP's are at least compatible to small minicomputers. The μP instruction set includes the standard logic and 2's complement arithmetic functions. Instructions are provided for I/O and interrupt functions. Flags are provided for sign, zero, and carry. Branches, calls to subroutines, and returns may be made unconditionally or by testing these flags.

Physically, μP's may come on one or several IC's. The first generation, as Intel's I4004, μP's have a 4-bit accumulator and require three or four IC's. The second generation, as the Intel I8080 and Motorola's MC6800, have 8-bit accumulators and are on one IC. There are others which are multiple chip and expand the accumulator in 4-bit increments. Also, Digital Corp. offers a PDP-8 CPU on an IC. Figure 1 is supplied as a reference point for size and chip counts in a basic μP computer.

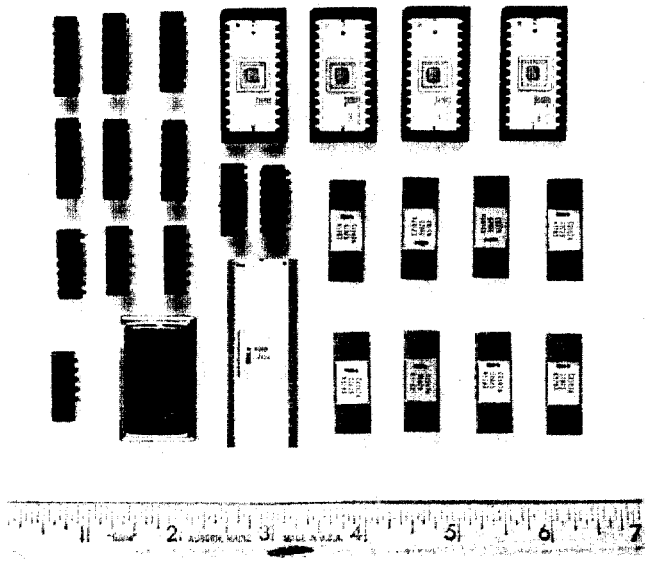

Fig. 1 μP computer with I8080 μP, 1K PROM, 4K dynamic RAM, crystal oscillator clock, and associated random logic.

Microprocessors and CAMAC

Fermilab developed a Type-U crate controller which interfaces to an I8080 μP.[1]

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The I8080 Type-U system[2,3] is a standard CAMAC[4,5] interface except for a topological change. The CAMAC crate, instead of being an appendage to the computer, hosts the computer on a CAMAC module. The block diagram in Figure 2 shows different features of this arrangement. The essential portion of interface, 8080 module and Type-U occupy three stations. The ensemble forms an inexpensive, portable, twenty-two station CAMAC computer system in a single crate.

The 8080 module uses the CAMAC crate only for power and as an enclosure, it does not connect to the dataway. The module contains an I8080, μP, 4K of PROM, 4K of RAM, I/O buffers, interrupt priority logic, and drivers for an external memory bus (EMB). The EMB is an extension of the I8080's address and data lines. All memory locations not local to the 8080 module are addressed to the EMB. This in effect creates an expandable bus which is used to interface to the environment.

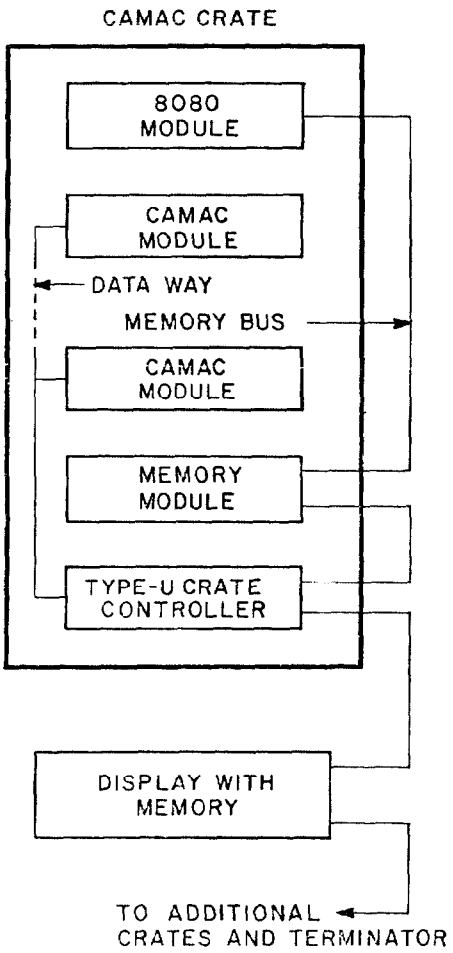

Fig. 2 Sample 8080 CAMAC system which illustrates extensions on the EMB.

Several examples of EMB devices are shown in Figure 2. The Type-U crate controller is a buffer between the EMB and the dataway. To the dataway, the Type-U looks like an A-1 or L-1 crate controller. To the 8080 module, the Type-U looks like a sequence of memory locations. Several Type-U's may be used to form multi-crate systems. Other examples of interfaces are the memory module which provides additional memory for the I8080 and the display which shares memory with the 8080 module and is not in CAMAC format. The EMB also has provisions for the external devices to cause interrupts. The system may be interrupt driven.

Applications and System Architecture

Autonomous Systems

An 8080 CAMAC system, 8080 module and Type-U controller is a standalone, autonomous system. Two applications of this will be shown. Figure 3 shows, as a first example, an interrupt driven system for data acquisition in a beam line experiment on radiation damage.[6] The target is a copper wire whose resistivity at cryogenic temperatures increases as it is bombarded. Data is gathered after each interrupt. The interrupts are generated by a special function module which decodes the experimental clock for proton burst times. The interrupts also cause the system to examine support equipment to be sure the data is valid. The resistivity measurement data and support equipment parameters are processed in the NIM crate for scaling to CAMAC A/D levels. A multipoint beam profile is collected from a split wire ion chamber (SWIC). Once gathered, the data is formatted and stored on a 9-track magnetic tape for later reduction and interpretation. The μP is used only as a data switchyard which is strobed by an external interrupt.

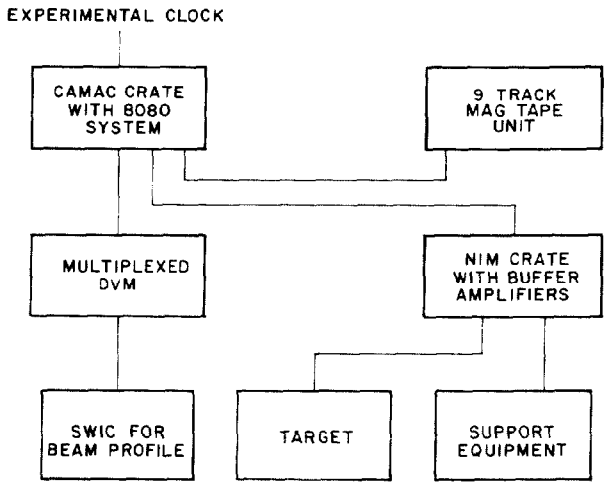

Fig. 3 Interrupt driven data acquisition system for beam line experiment.

Another example is shown in Figure 4. In this system, the I8080 μP not only logs monitors and data, but it controls the process. The experiment[7] is a repetitive measurement of low temperature thermal conductivity. The CAMAC system controls the experiment by setting reference voltages with D/A modules. The data is collected from the NIM buffering and processing electronics into CAMAC A/D modules.

Permanent storage is on paper tape. The sequence of the experiment is initiated by setting the temperature controller to the experimental temperature. A second heater is then set to a proper temperature difference for the measurement. The μP then monitors the temperature variations versus a real time clock on a CAMAC module. When the μP determines that experiment is at thermal equilibrium, it logs, reduces and outputs the data to the teletype. Then the cycle begins again.

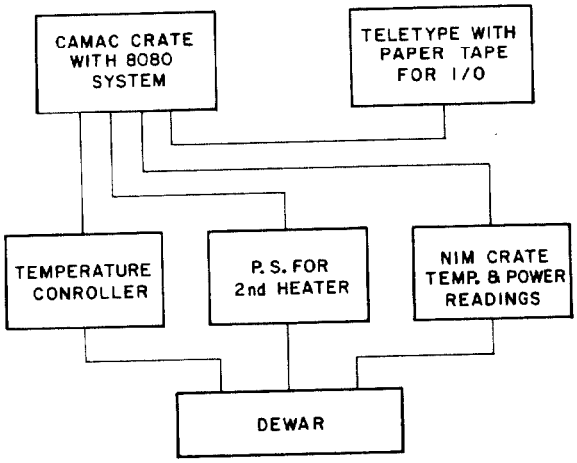

Fig. 4 Real time process controller for laboratory equipment.

Distributed Systems

A distributed computer system consists of two or more distinct computers sharing computation and operation of a common task. This distribution of the operation and computation may be made on several bases - physical separation, division by logical blocks, and optimizing the strengths of each computer.

A system divided by physical and logical blocks is shown in Figure 5. The multi-crate 8080 system is physically part of the power supply ensemble[8,9] (PS1, PS2, and PS3). The 8080 and auxiliary crates assume the monitoring and control of supplies. Also, it performs the logical function of collecting the local keyboard data and operating the display.

The network computer (not shown) is only responsible for providing the four times for the power supplies to pulse. This arrangement relieves the network computer of any real time responsibilities as checking interrupts before each pulse, monitoring waveforms, or switching loads and power supplies used on each different pulse. Also, the network computer does not have to collect data from the power supply assembly just to return it to a local display. The network computer controls the only parameters of interest to its system - pulse times. This type of interface is implemented with a pseudo module. A pseudo module behaves as any special function CAMAC module from the view point of the network computer, but transmits the twenty-four bits of the dataway operation to a receiving module in the 8080 system which can read and use it as an input. This requires no special software on the part of network computer.

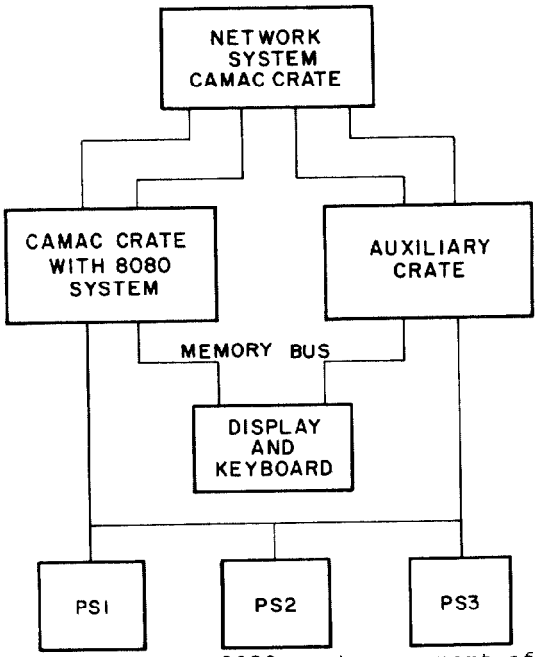

Fig. 5 Two crate 8080 system as part of power supply ensemble and distributed computer system.

The distributed system in Figure 6 is a generalized primary computer to CAMAC interface.[10] The portability of software and hardware between different models of primary computers was emphasized. The communication between computers occurs at two levels - I/O and DMA. The primary computer and 8080 system transfer information bi-directionally off the primary computer's I/O bus. High speed commerical CAMAC modules are available to do this. The 8080 system cannot distinguish one computer from another at this level. The primary computer can treat the CAMAC module as a standard I/O device. The bi-directional DMA link is a little more specialized. It has to be designed for a particular computer, but it simple and inexpensive. The difference in primary computer DMA channels is accounted for in buffer module hardware and the I8080 never sees the difference. The software in the primary computer now needs to know less about CAMAC and the machine and retains a greater computer independence.

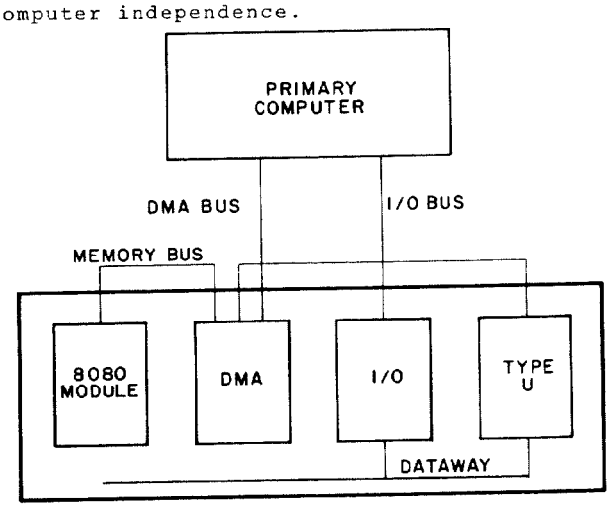

Fig. 6 Generalized computer to intelligent CAMAC crate interface.

The distribution of computation and operation is by optimization. The strength of the primary computer lies in its computational power and access to peripherals such as disk and magnetic tape. The primary computer can reduce the data collected by CAMAC, compile and assemble I8080 programs and store them on disk. The I8080 can respond as real time process control taking care of all the small details that do not require a lot of computation.

Conclusion

Microprocessors are useful tools in accelerator equipment. They can be used in applications where the expense of minicomputers cannot be justified or are not needed. They can also be used to expand the capabilities of existing computer systems.

Acknowledgement

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