PRIMET: A VERSATILE ACCELERATOR TIMING SYSTEM

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Introduction

The control systems at NAL extend over distances in excess of 10 miles. In order to synchronize machine events, not necessarily time related, it is essential that the same timing information be provided to all areas. Various methods of implementing a timing system which would provide accelerator event reference times were considered. In our application, a single line clock transmission system, using a serial encoding feature, proved to be the most economical and practical. It is easy to implement, reliable, and provides versatility while maintaining a degree of simplicity. All that is required to transmit this encoded clock to different areas of the accelerator are clock repeaters and a single cable. In general, the encoded clock is connected to either computer or manually controlled timing modules which act as preset counters. The serially encoded information is selectively detected by these modules and used as accelerator event reference times. Any one of 14 reference times can be used as a timing pulse or as a start signal to the module, which then produces a pulse delayed from the selected reference by a predetermined amount of clock counts.

Master Clock Generator

The Master Clock which is used as a source for the encoding process is a nominal 1 Megahertz oscillator which is synchronized to the 60 Hertz line voltage provided by Commonwealth Edison. This feature is necessary since the accelerator is operated directly from the line and this clock is used to program the Main Accelerator power supplies.

The Master Clock is composed of a counter, D/A (digital to analog converter) and a VCO (voltage controlled oscillator), as shown in Figure 1. The clock operates in a closed loop where it receives update information synchronized to, and at a 60 Hertz rate. Since the clock is slaved to the line period, its frequency will change if the period of the line frequency changes. When the period changes, error counts will be strobed into the D/A at the 60 Hertz update time. The analog voltage output of the D/A changes the frequency of the oscillator by changing the voltage at the input to the VCO. Since the counter is not cleared, and the counts shown in Figure 1 for nominal 1 Megahertz operation remain the same, errors accumulate. This error however, is progressively driven toward zero by the 60 Hertz update. The effect of this type of operation is that over long periods of time no counts are lost. As the line period changes the damped response of the loop slowly and continuously maintains the nominal 1 Megahertz frequency.

Phase Reversal Generator

The method used to serially encode information into the Master Clock pulse train is termed phase reversal generation. PRIMET (Phase Reversal Interval for Machine Event Timing) is used to encode up to 14 phase reversals (P.R.'s) or reference times into the Master Clock pulse train. This type of encoding is not limited to 14 but was chosen for practical as well as technical reasons.

A reference time having three phased reversed cycles of the clock is shown in Figure 2a and 2b. As can be seen in these figures, the clock signal consists of ±10V bipolar pulses. The negative pulse is generated 250 nsec after the positive pulse from the Master Clock. The 2 Megahertz pulse rate is used to shorten the detection time. One cycle of the clock is defined as one positive pulse followed by one negative pulse. Using this definition the clock can be thought of as having a frequency of 1 Megahertz. The timing modules which use this clock actually count only the positive pulses providing a maximum resolution of 1 μsec.

Figure 2a shows the normal pulse train just before and just after the three P.R.'s. Figure 2b is an expanded view of Figure 2a. The second adjacent negative pulse, shown in Figure 2b is the start of the P.R. time interval. The following three cycles are what is termed a P.R. of three. The second adjacent positive pulse shown in Figure 2b signifies the end of the P.R. interval, after which, normal clock generation is as shown in Figure 2a.

Detection of this particular reference time uses the second adjacent negative pulse to enable a counter. The positive pulses are then counted until the second adjacent positive pulse occurs, disabling the input to the counter. At this time a count of three exists in the counter. At the end of the P.R. interval the number in the P.R. counter is compared with a number stored in a latch and an output pulse is generated if an equality exists. The same method is used to detect all other reference times.

A block diagram of PRIMET is shown in Figure 3. A 15 input latch is connected to a priority encoder which develops a BCD code of the input. All 15 inputs act as interrupts to the P.R. generator. The highest priority P.R. is the one P.R. interval. If two or more inputs occur simultaneously the one serviced first will be the lowest numbered.

The P.R. counter is loaded with the BCD code from the priority generator by the strobe from the OR gate. This starts the generation of the selected P.R. When the proper number of P.R.'s have been executed, the end of P.R.

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* Operated by Universities Research Association Inc., under contract with the U. S. Atomic Energy Commission.

generation pulse will test for any existing interrupts and clear the previous interrupt just serviced. If no other interrupts exist the generator outputs the clock with no P.R.'s.

There are actually two modes of operation used in the generator because of certain Main Accelerator cycle reference times. A typical Main Accelerator waveform is shown in Figure 4. T1 through T6 are reference times which mark particularly important reference times in the cycle. They also correspond to the number of P.R.'s that are generated at those particular times. These reference times are very important and cannot be affected by any other time reference produced as a P.R., hence the two modes of operation.

These two modes are termed Normal and Protected. The Normal mode is one in which the reference time is not one of prime importance. The Protected mode, used for reference times as shown in Figure 4, delays both the start of P.R. generation and the test for new interrupts by 32 μsec. This is done to prevent the shifting in time of a protected reference if a normal P.R. other than that shown in Figure 4, is being generated when the Protected P.R. interrupt is received. When a Protected P.R. interrupt occurs during a normal P.R. the delay counter is started. Since the longest P.R. generation time is 14 μsec and the counter delays Protected P.R. generation for 32 μsec, a conflict of time cannot occur. Overlapping operation of Normal P.R. generation and the start of the delay counter for the Protected mode, prevents time jitter of the protected reference times. There are 8 Protected reference times out of the 14. The remaining six can be used as general purpose reference times. An interrupt can occur at any time and the reference time will be generated according to the previously stated priority.

The clock is transmitted as a bipolar pulse train using transformer coupling at all repeating and receiving modules. Transformer coupling is used for isolation and to improve noise rejection on the clock lines.

The hardware involving the generation of the P.R.'s is shown in the photograph in Figure 5. The P.R. generator uses a two wide panel module in the CAMAC crate. Complete testing of the generator can be done from this front panel. A hexidecimal display shows the gap just produced. The panel above the CAMAC crate is the input trigger panel into which timing pulses (interrupts) are connected to produce P.R.'s. This affords complete freedom in the assignment of P.R.'s with regard to number and priority.

General Operating Features

The reference times as shown in Figure 4 are encoded in the clock at specified times either by real time interrupt triggers, or by interrupts generated by machine operation. The real time triggers are obtained from timing modules which use the 1 Megahertz line-locked Master Clock. Examples of protected reference times which use real time triggers would be the Main Ring reset (highest priority), start of Rectification, Flattop, etc. as shown in Figure 4.

A requirement for a reference time which is not time related, is one which must be generated when the Main Accelerator and Injector are in synchronism for beam injection. The beam momentum in both machines must be the same, Injector beam must be in the proper radial position and the selected empty buckets in the Main Accelerator must be in position to accept Injector beam. When all these conditions are met, the synchronizing electronics provides an interrupt pulse to the P.R. generator. This reference time can then be detected and used to initiate the injection of beam into the Main Accelerator.

Another application of a reference time is one in which a variable time trigger is connected to produce a specific phase reversal anywhere in the accelerator cycle. As this trigger is moved from a reference point, say M.R. reset, the encoded phase reversal also moves. An operator, by twirling a knob on a Main Control Room console, can move a phase reversal through the entire Main Ring cycle. This type of operation could be used where a general reference time is needed when the exact time of an event is not known.

The clock is distributed throughout the beam lines using pulse repeaters located in CAMAC controllers. Manual or computer controlled modules in these controllers are used to detect the reference times and produce timing pulses. The modules can be used to detect any of the 14 reference times. Once a timing pulse has been produced from a module it clears itself and will not produce another pulse until the reference time that had been selected occurs again. It is possible that a particular reference time will not be generated every machine cycle. This could, for example, occur when a reference time is used to indicate whether or not beam is being accelerated. In this case the detection of the reference time would trigger equipment only when beam was actually available.

Beam Line Equipment

There are three types of timing modules used to detect reference times in the beam lines. The CAMAC clock fanout, the CAMAC timing module and the PREDET are shown in Figure 5. Each module receives and decodes the incoming clock as previously explained under the heading "Phase Reversal Generator".

The clock fanout module receives the incoming bipolar clock and generates three buffered outputs. It is used to provide multiple outputs at a control station. It detects all 14 reference times, of which 4 can be selected as outputs on the front panel. A LED associated with each output indicates the presence of an output pulse.

The CAMAC timing module is computer controlled. The computer writes a 24-bit word into a register of the module. The most significant 4 bits are used to select one of the 14 reference times. Writing a zero into the reference time register will inhibit both the time reference and the delayed outputs. A front panel inhibit switch is also provided

for this purpose. Writing a one into the reference time register allows an external pulse from the I/O connector to be used as an external reference. The remaining 20 bits specify the desired time delay at 10 μsec per count with respect to the reference pulse. There is a buffered bipolar clock output available for daisy chaining modules.

The PREDET is a manually settable timing module which can be used either in a CAMAC crate or in a NIM crate. There are four independent sets of 5 digit thumbwheel switches which are used to set the time delay from the selected reference. A 16-position thumbwheel switch on the front panel selects INHIBIT, EXTERNAL pulse reference, or any one of the 14 reference times. A 3-position switch selects 1 μsec, 10 μsec or 100 μsec per count of delay. Three LED lites are provided for displaying the current selection. All pulse outputs can be hardwired to either NIM or logic or T^2L logic levels. The output characteristics in either case is a pulse 1 μsec wide driving 50 ohms.

Acknowledgments

The authors would like to thank Gary Solomon, Santo Lamantia, Richard Dice, and Thaddeus Ulijasz for their effort in fabricating and testing the equipment presented here.

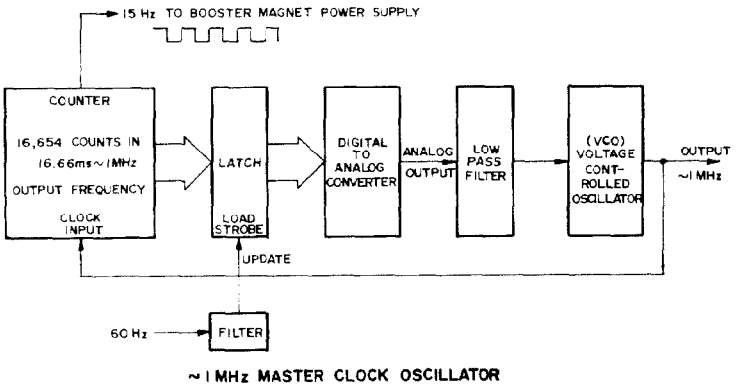


Figure 1.

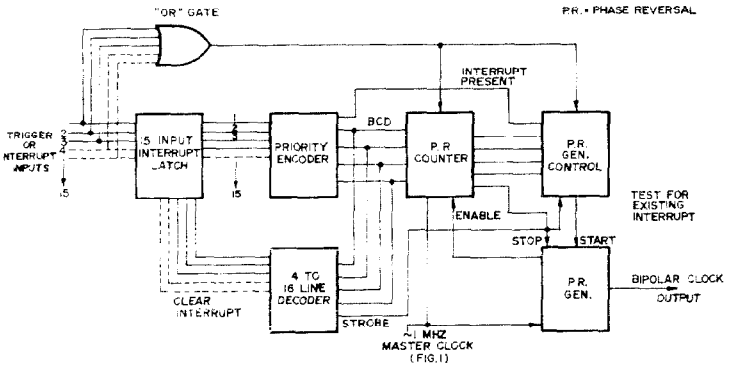


Figure 3. Phase Reversal Generator.

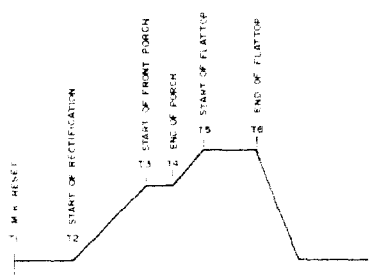
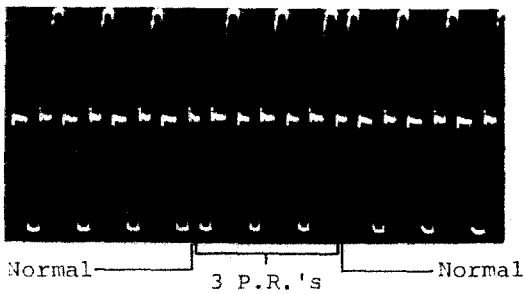
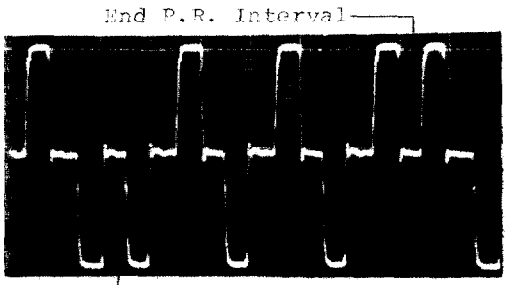


Figure 4. Main Ring Waveform.



Vert. = 5V/DIV
Horiz. = 1μs/DIV

Figure 2a.



Vert. = 5V/DIV
Horiz. = .5μs/DIV

Figure 2b.

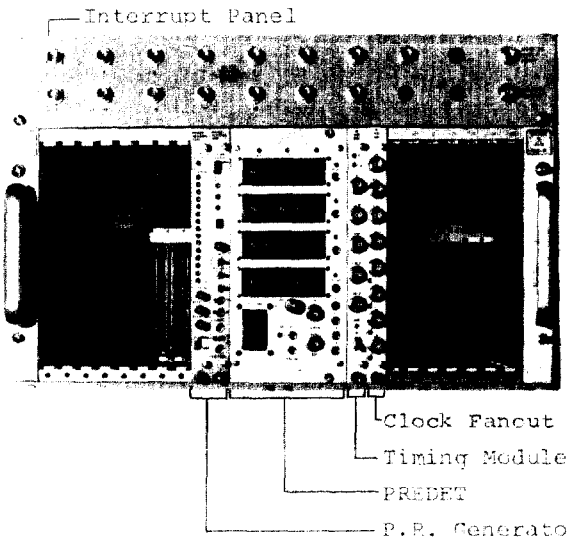


Figure 5.