I.U. ACCELERATOR CONTROL SYSTEM DIGITAL MULTIPLEXER*

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Summary

A digital distribution system has been constructed at the Indiana University cyclotron facility to link the control computer, an XDS Sigma 2, with the three stages of the accelerator and the control console. This system consists of a network of modular digital multiplexers attached to a common bidirectional data bus. When fully expanded, the system can transmit or receive 16-bit data words to or from 1024 different devices. In addition, a device may generate a computer interrupt by raising 1 of 256 available status bits. The multiplex system was implemented with XDS T series modules and thus is compatible with any DTL or TTL logic.

Introduction

To link the accelerator and control console to the computer, an XDS Sigma 2, a digital multiplexer network capable of switching up to one thousand 16-bit input and output data words has been constructed. Although the design is relatively straightforward, several alternatives for implementing it were considered. These alternatives included: building the multiplexer from logic modules built in-house, building the multiplexer using commercially available logic modules, and building a multiplexer based on CAMAC hardware. Manpower and time considerations eliminated the first alternative. A cost analysis revealed that a system built from commercial logic modules would cost only about two-thirds that of a system built from CAMAC hardware. This fact, coupled with the knowledge that we could have our logic bins commercially wire-wrapped for a small fee, led us to choose the second alternative for implementing the multiplexer design. It should be mentioned, however, that although we decided against using the CAMAC approach for the multiplexer and, as a result, the control system, CAMAC is being used for the experimenter's data acquisition system, where the main criteria are flexibility and uniformity to the user.

Multiplexer Description

The design of the multiplexer was based mainly on two criteria. First, the system was to be attached to the Sigma 2 Direct Input/Output (DIO) interface. The DIO interface provides 16 address lines, 16 bidirectional data lines, and a function strobe (FS) line. Additional signals provided include a read/write signal, a reset signal, a 1.024 MHz clock signal, and two lines for inputting status information. Several lines for producing internal interrupts are also available.

The second criterion was that the system be modular in nature and capable of decentralization. By developing a few standard units, the design and construction costs were minimized. Although the expenditure necessary to check out the system was modest, the system may be expanded almost indefinitely as the need arises. Decentralizing the system reduces signal cable lengths, thereby minimizing noise problems and cabling costs. In addition, it avoids the congestion that would be produced by bringing all of the cables together at a central location.

As can be seen from the block diagram shown in Fig. 1, the multiplexer system is built from three basic units. Each control unit can handle a maximum of eight read units and sixteen write units. Each read unit contains sixteen 16-bit input gates for inputting data to the computer. Each write unit contains eight 16-bit storage registers which hold data sent out by the computer. Thus, a total of 128 16-bit bidirectional data words can be handled by each control unit. Up to eight control units may be implemented, each, if desired, at a different location, so that the system can be expanded to randomly address up to 1024 16-bit digital input words and 1024 16-bit digital output words.

In addition to providing means of inputting and outputting data, the multiplexer contains sixteen 16-bit status registers, two located in each control unit. The outputs of all status registers are "OR"ed together to an interrupt line. Thus, when an external device requires service, it simply raises its status line, which causes a computer interrupt. The computer then interrogates the status registers to determine which external device requested service and takes appropriate action.

In designing the status bit circuitry the major obstacle encountered was that of remembering status signals that were generated while the computer was interrogating and resetting the status bit register in response to an earlier status signal. The circuit shown in Fig. 2 solves this problem. The basic circuit consists of a NAND gate latch, an AND gate, and a NOR gate latch. With a "0" input, the NAND gate latch will be set (Q_A=1) and the NOR gate latch will be reset (Q_B=0). When an input goes high, the level will pass through the AND gate and set the NOR gate latch (Q_B=1). The setting of this latch triggers the interrupt and also resets the NAND gate latch (Q_A=0). The resetting of this latch prevents retriggering of the computer interrupt line by the same signal after the computer has read and reset the NOR gate latch. The GATE signal is normally high and only goes low during the reading and resetting sequence, an operation taking about one microsecond. When the GATE signal is low the NOR gate latches are isolated from the inputs and cannot be set by incoming signals. However, as soon as the GATE signal goes high again any new signal present at an input will cause the NOR gate latch to be set. To avoid missing any interrupts, the duration of the input signal must be longer than the time the GATE signal is low. The GATE and RESET signals are obtained from one-shots that are triggered by the function strobe signal that is generated when the computer is ready to read the register.

Another feature incorporated into the multiplexer is a "watch-dog" timer. All devices connected to the multiplexer must raise a function strobe acknowledge (FSA) line when addressed by the computer. If the FSA is not raised within a certain time limit, the FSA line is automatically raised by the timer. In addition, a status line is raised which indicates that the addressed device did not respond.

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Multiplexer Implementation

The major portion of the multiplexer design was implemented with XDS T series logic modules. These modules feature positive level logic, where 3.6V dc to 10V dc represent a "TRUE" or logic "1" and -3V dc to +1V dc represent a "FALSE" or logic "0". These characteristics must be met by all external devices connected to the multiplexer. Another feature exhibited by these modules is their high output loading capability. External devices may be installed up to 100 ft. from the multiplexer without the need for special driver-receiver circuits.

The status bit circuitry was developed using T^2L integrated circuits. Although T series modules could have been used, lack of space in the control unit would have necessitated the use of another bin. Therefore, a special board, the same physical size as the T series modules, was developed. Each of these boards contain the circuitry for eight status bits.

Data communication between the computer and the multiplexer is via three 14-conductor miniature coaxial cables. In addition, a fourth cable is used for direct connection to the Sigma 2 integral priority interrupt chassis. These cables are supplied by XDS. External devices are connected to the multiplexer by means of a cable containing 19 twisted pairs. The cable is terminated on a special card for which provisions have been made in the multiplexer. All modules are mounted in pre-wired mounting cases. These cases are automatically wire-wrapped by XDS from computer-generated wiring lists.

Conclusion

The first multiplexer station was put into operation about two years ago and the second station about one year ago. During this period of time many devices such as ADC's, DAC's, encoders, stepping motors, relays, and lamps have been interfaced to the computer via the multiplexer. Operation during this period of time has been virtually trouble free. Enough units have recently been ordered to assemble three more stations. These three stations, along with the two stations now in operation, will suffice to handle the control requirements of the three stages of the Indiana University accelerator.

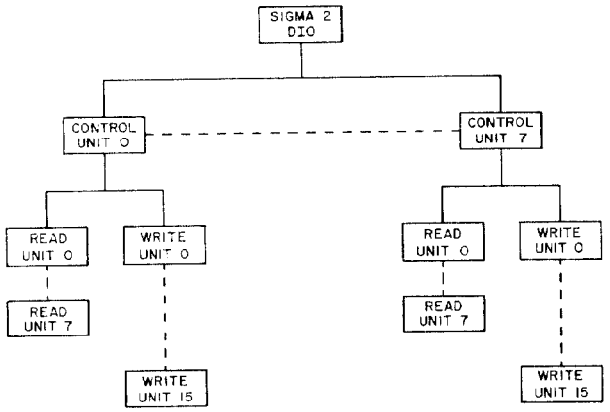

Fig. 1. Multiplexer block diagram.

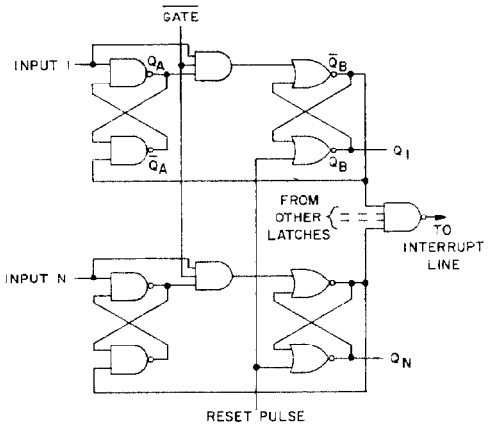

Fig. 2. Status bit logic.