BOOSTER AND MAIN ACCELERATOR PHASE DETECTOR SYSTEM FOR CAVITY TUNING

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Summary

Each NAL booster and main accelerator rf station contains a phase lock control loop to resonate the beam-line cavities at the applied excitation (reference) frequency.

The phase sensor in the loop is a dual channel phase detector having an octave bandwidth, an amplitude dynamic range of 60 dB, a phase balance vs. frequency better than ±2° and a zero crossover phase sensitivity of 0.18 V/deg. The phase detector develops a feedback "error" signal proportional to the phase difference between the rf reference signal and an rf signal representing the rf station beam line voltage.

This paper discusses the rf cavity tuning feedback loop configuration and describes the details of the phase detector circuitry.

Phase Lock Loop

Figure 1 shows a typical high level rf station cavity tuning loop. The configuration is essentially the same for both the booster and main accelerators. Each beam-line cavity is adaptively tuned to the rf reference frequency during an acceleration cycle by the elements shown in the control loop.

The reference rf signal is developed for each machine by separate voltage controlled oscillators within tracking loops conditioned by computer generated tables of df/dt and/or by direct beam-dependent inputs. The rf reference signals are distributed to the power amplifiers by 16-channel fan-out systems which contain phase equalization networks to establish specific rf phases at each station. The beam-line cavities shown in Figure 1 are excited by rf power amplifiers developing as much as 100 kW of rf power. These cavities are tuned by controlling the magnitude of the biasing current supplied to ferrite-loaded tuners physically attached and electrically coupled to each cavity. A 2,500-A programmable bias power supply, one for each rf station, functions as a driver for the tuners.

The phase detector in the control loop receives an rf signal from an ANODE monitor port on the power amplifier, representing beam-line phase, and a CATHODE monitor signal, representing the reference phase. These signals vary over wide limits in amplitude and vary in frequency, depending on the machine, throughout the range from 30-53 MHz. Phase equalization of the distribution system, however, establishes phase coincidence of the detectors ANODE and CATHODE monitor inputs when the beam line cavity resonant frequency matches the reference frequency. Since the ANODE monitor signal is derived from a Hi-Q selective circuit (the beam-line cavity) its phase response in the band of interest exhibits a single "zero" at the point of cavity resonance. The phase detector, a sine-law processor, thus produces an "error" voltage which is odd about the "zero" phase response point and proportional to $\sin\{\arctan[2QS]\}$ where Q is the resonant circuit Q and S is a frequency variation parameter, $(f_{reference}/f_{cavity}-1)$.

The detector developed "error" voltage is filtered, combined with an analog function representing the best estimate of frequency during programming, and is returned to the programmable bias supply to complete the loop.

The dynamic properties of the control loop are set mainly by a loop filter having a transfer function, F(s), of,

$$F(s) = \frac{(2.27\times10^{-4}s+1)(4.45\times10^{-4}s+1)}{(2.26\times10^{-2}s+1)(7.78\times10^{-6}s+1)} .$$

This filter provides phase lead to extend the loop cut-off frequency while maintaining stability and allows little attenuation at low frequencies thereby improving the dc error coefficient. The open loop dc gain of the system is about 45 dB. The unity gain crossover slope is -9 dB/octave and occurs at about 3 kc.

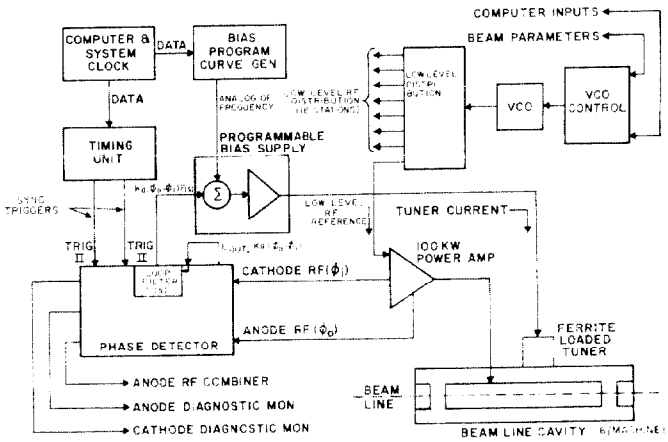

Fig. 1. Cavity tuning phase lock loop.

Phase Detector

Description General

Figure 2 shows the phase detector system block diagram. The figure shows the major modules, input, output, and trigger connections, and designates specific voltages for referral in the detailed circuit description.

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The detector system consists of a set of rf input signal coupling devices, two independently regulated gain controlled rf channels, a phase sensitive demodulator, an error signal multiplexer, and various regulated dc supplies to power all circuits.

The input coupling devices provide the means to match the ANODE and CATHODE rf signals to the detector input circuits, and establish the rf signal operating point by fixing the upper rf level inputted to the (AGC) amplifier.

Through the characteristics and the control action of the rf amplifiers, the phase detectors transfer function is made essentially independent of the AM and FM present in the rf input signals. AGC control action makes the AM effects negligible, while carefully matching the absolute gains and rf phases of both AGC amplifier channels secures independence from FM error effects.

The phase demodulator develops an error voltage related to the sine of the phase difference between the ANODE and CATHODE channels. The phase "error" voltage is produced by differencing the rectified voltages at the output-side of a multiport broad-bandwidth lumped-element hybrid junction. The phase error voltage is amplified and applied to an analog multiplexer for further processing.

The multiplexer amplifies the phase demodulator output signal and controls the period of time during which the amplified phase error signal is applied to the cavity tuning control loop. Specifically, multiplexer switching action applies the phase error signal only during each active acceleration cycle, while inhibiting the signal during the cycles dead-time interval. In this way the multiplexer prevents noise or spurious signals from influencing the tuning control loop prior to the start of follow-on active cycles. In addition, the multiplexer module allows externally applied voltages to control the tuning loop during the dead-time interval.

Description Detailed

ANODE and CATHODE Signal Splitters. The ANODE and CATHODE rf signals enter the phase detector through 3-way reactive-hybrid junction signal splitters. These splitters are designed for 50-ohm service and furnish isolated rf samples to local viewing ports at each rf station and to level set attenuators RF-1 and RF-2 (Figure 2). The ANODE splitter at each rf station transmits a sample for diagnostic purposes to a 16-channel multiport combiner which produces a voltage proportional to the total active-cycle rf voltage. The hybrid signal splitters, throughout the 30-to-53 MHz range have voltage coupling factors of -4.8 dB, port-to-port phase error less than 1°, phase tracking error vs. frequency less than 1°, amplitude balance between ports better than 0.5 dB, and isolation between ports of more than 30 dB.

RF-1, RF-2 Attenuators. Level set attenuators RF-1, RF-2 produce attenuation with very small inherent phase change. These units permit the phase detector input signals to be adjusted independently. Attenuation is produced by rotational displacement of two coils wound on facing ferrite half-cores. The angle made between the half-cores is mechanically adjustable, but the spacing between cores is fixed. The amplitude transfer function of the attenuators is related to the rotation angle θ, the smaller angle between core axes, and core spacing. The function is

$$V_{rf\ out} = \frac{V_{rf\ in} \cos\theta}{10} \text{ volts.}$$

The output phase angle varies less than ±1° over the 20 dB continuous adjustment range. The attenuators are paired so that the insertion phase vs. frequency tracks within ±1.0° throughout the operational band.

AGC-rf Amplifier. The AGC rf amplifiers contain low gain variable transconductance amplifying stages having matched gain and phase characteristics. Each amplifier is gain-controlled by a feedback arrangement which controls the gain over a minimum range of 40 dB. The CATHODE and ANODE signal channel AGC amplifiers are matched in gain to ±1 dB while the phase difference between channel amplifier is held to less than ±1.5° for all gain settings. Two control stages having unity maximum gain, and contributing 20 dB to the total dynamic range, together with a 3-stage solid state interstage amplifier with adjustable feedback are employed in the design of the AGC amplifiers. The interstage amplifier provides 30 dB of isolation between control stages and permits the trimming of both gain and phase for matching purposes. The gain control signal spectrum, dc-to-3 MHz, is attenuated by more than 50 dB by frequency selective coupling networks.

AGC/FGC Gain Control Circuits. The AGC control system used for each rf channel consists of two tandem connected regulators. The first regulator is a conventional closed-loop feedback circuit with a closed loop gain of 26 dB. This loop provides the major part of the regulation. Figure 3, lower, indicates the regulation characteristic associated with this circuit. The rf output from the first regulator is reregulated by a narrow range, 3 dB, fine gain corrector (FGC) circuit,

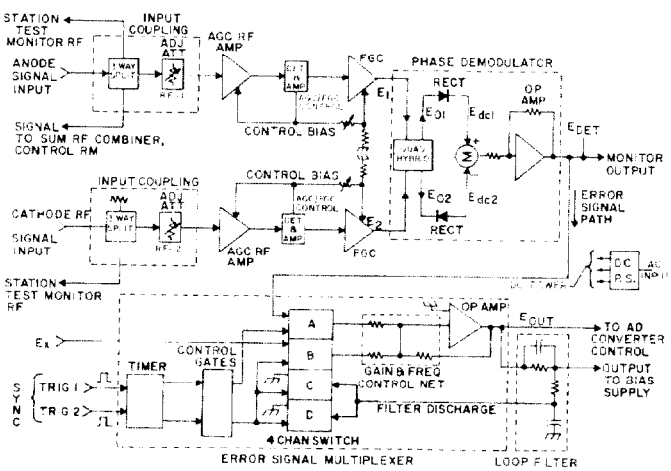

Fig. 2. Phase detector block diagram.

which is activated by a fed-forward fraction of the first regulators control bias. The combined performance of both regulators is shown in Figure 3, upper curve. The effective loop gain of the regulators is greater than 35 dB. The overall speed of response of the AGC/FGC gain control system is 10 dB/μsec.

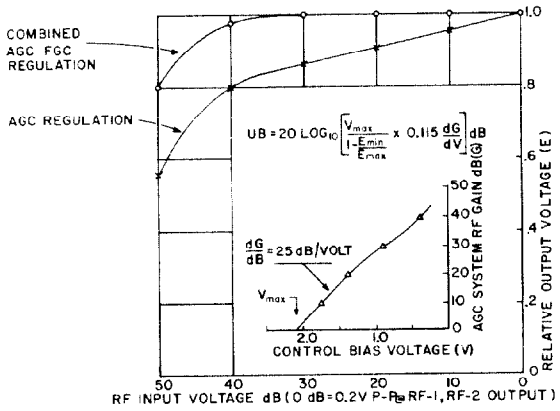

Fig. 3. AGC regulation characteristics and gain vs. bias relationship.

Phase Demodulator. The phase-demodulator consists of a quadrature hybrid 4-port, a proportionally biased difference rectifier, and an error-signal amplifier. The quadrature hybrid is used to convert phase modulation at its input terminals to amplitude modulation at its output terminals. The quadrature hybrid rf input phasor signals, $E_1 = E_2 = E_{in}$, Figure 2, are made equal in amplitude by AGC, have the same frequency, but may assume a phase relationship within bounds dictated by cavity/reference frequency difference (±90°). The amplitude of the two output signals, E_{01} and E_{02}, are related to the rf input signals and the input phase difference angle (ϕ) by

$$E_{01} = E_{in}\sqrt{1+\sin\phi} \qquad \text{and} \qquad E_{02} = E_{in}\sqrt{1-\sin\phi}.$$

Since the E_{in} component in the above expressions is kept constant, the phase ϕ is the variable responsible for the output error signal. The quadrature hybrid output rf signals, E_{01} and E_{02}, are applied to a matched pair of PIN diodes, connected so as to produce an output voltage proportional to the difference in peak-rectified voltage. With this connection and for rf inputs below 1-V P-P, the diodes operate in a region which is essentially "square law." The dc voltage at the load side of the diodes is

$$E_{dc1} = K_1\left[E_{in}\sqrt{1+\sin\phi}\right]^2; \quad E_{dc2} = K_2\left[E_{in}\sqrt{1+\sin\phi}\right]^2$$

where the detector constant $K_1 = K_2 = 0.3$ and $E_{in} = 0.4$ V-P, nominal.

The difference of the rectified voltages, (Edc_1 - Edc_2) is amplified by a factor of 20 and filtered to give a detector output signal, (Edet), of

$$Edet = \frac{2\sin\phi}{1+0.2\times10^{-6}s} \text{ volts.}$$

The zero crossover phase error versus frequency for applied equal amplitude and in phase voltages is less than ±2°. The zero crossover sensitivity at the demodulator output is .035 V/deg.

Error Signal Multiplexer. The multiplexer time shares the phase demodulator developed error signal with an externally applied function through port E_X, Figure 2. Control triggers TRIG-I and TRIG-II, timed to coincide with the beginning and end of each booster or main accelerator cycle activate the multiplexing circuits. TTL integrated circuits as well as discrete semiconductor circuits develop synchronized bipolar control gates which are applied as drivers to a quad-bilateral analog switch (RCA 4016A). Two channels of this switch are used to transmit alternately the phase error voltage and the externally applied analog function (E_X) to an operational amplifier combiner; thus forming the multiplexing action. The nominal transfer function for the error voltage at the Eout port, during the active accelerator cycle, is

$$Eout = \frac{10\sin\phi}{(1+2.0\times10^{-6}s)\ (1+0.2\times10^{-6}s)} \text{ volts.}$$

A typical plot of the output voltage vs. phase difference angle is shown in Figure 4. The sensitivity at crossover is 0.18 V/deg. For the externally applied voltage, the transfer function during dead time is

$$Eout = \frac{Ex}{1+0.2\times10^{-6}s} \text{ volts.}$$

The remaining two channels of the analog switch discharge the loop filters storage capacitor.

The separation between the error and E_X channels is typically greater than 35 dB, while switching transients are less than 0.05 volts peak and last less than 1 μsec.

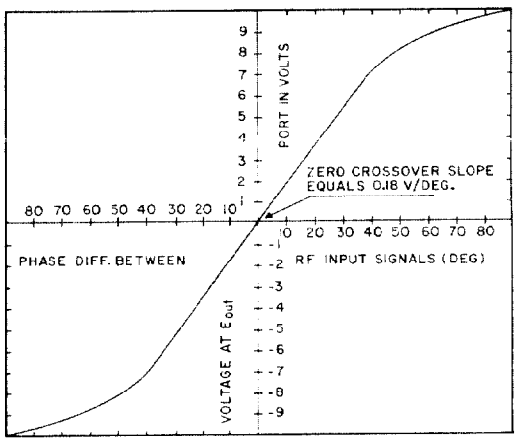

Fig. 4. Phase detector output voltage vs. RF phase difference.

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