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AN ALL SOLID-STATE LINE-TYPE MODULATOR FOR 10% DUTY FACTOR

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Summary

IKO has recently obtained approval of its proposal to build a high duty factor linear accelerator. Main characteristics of this machine: 500 MeV at 2½% and 250 MeV at 10% d.f. R.F. power is to be obtained from 12 klystrons (100 kW av., 1-6 MW peak). A prototype modulator has been constructed. It consists of 48 modules, each of which is a printed circuit 2 kV line-type (50 µs) modulator. Each module feeds a primary winding of a special pulse transformer, in order to supply the 160 kV max. video pulses for the main klystron. The modulator lay-out allows the provision of video pulses, the amplitude of which can be regulated on a pulse to pulse basis with a special purpose processor. Cooling is achieved through the liquid vapor phase change of freon. Details of the system will be given together with first test results.

Introduction

Fall 1972 IKO obtained approval from the Dutch Government for the construction of a high duty factor linear accelerator. The main requirements on beam specifications of this machine: nicknamed MEA (Medium Energy Accelerator) are:

Table 1: Beam parameters

Electrons	
Energy	50-500 MeV
Intensity	max. 1 mA average
Repetition rate	2000 pps max.
Pulse duration	50 µs
Duty factor	0.025 at 500 MeV
	0.1 at 250 MeV
Beam power	max. 250 kW
ΔE/E	0.1% for 50% of I_{max}
Secondary beams	Photons
	Neutrons
	Pions
	Muons

The beam center line components have been designed following the lay-out of the MIT 400 MeV machine. The injector, accelerator sections and klystrons will be ordered from manufacturers. All peripheral equipment will be constructed in house. Since some years, special effort has been made to design an all solid-state line-type modulator which fulfills the specific requirements for the high duty cycle performance of the accelerator. Report on that design and the present status of the constructed prototype modulator, which under test now, will be given below.

The total r,f, power needed to achieve the beam energy will be delivered by 12 klystrons. The main klystron characteristics are listed in table 2.

Table 2: Klystron specifications

Frequency	2856 MHz
RF power output	6 MW peak, 100 kW av.
Collector dissipation	350 kW
Video duty	0.12 max.
Video pulse width	60 µsec max.
Efficiency	30-35%
Gain	40-47 dB
Phase sensitivity	$7-10^{0}$/1%
Amplitude sensitivity	3.5%/1%

The adjustable electron beam energy can in principle be obtained by means of the following methods:

1. On-off control of one or more modulators working at a fixed power level (in use at SLAC). This will results in gross energy changes if only a small number of modulators is available.
2. Continuous control of klystron video power (in use with most linacs). A disadvantage of this method is the added requirement of continuous control of the phase and amplitude of the drive power.
3. Shifting the phase of the RF power with respect to the phase of the electron beam (mostly used in conjunction with methods 1 and 2.

We have chosen a combination of the three methods. Each modulator can be operated at 4 different RF peak power levels (1, 2, 4 and 6 MW). Fine adjustment of the RF phase is achieved through control (+ 3%) of each level. Gross phase corrections will be obtained by means of digital RF phase shifters at drive power level.

Simultaneous execution of different experiments requires machine operation on a pulse-to-pulse basis. If the klystron voltage is to be varied within 400 µsec, serious difficulties arise due to the changing klystron impedance (line-type modulators) and rapid adjustment of the power supply (hard-tube modulators).

Excellent pulse specifications have been obtained with the MIT hard-tube modulators. IKO however decided to develop a special all-solid-state line-type modulator for the following reasons.

1. The solid-state components used for the home built modulators for the present 85 MeV linac have demonstrated excellent performance.
2. Longer-lifeexpectancy of solid-state devices than high power vacuum tubes.
3. Lower cost price and lower maintenance costs.
4. Improved techniques to obtain sufficiently good beam specifications from line type modulators.

Since a number of specific problems related with solid-state line-type modulators had to be studied in more detail, it was

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decided some years ago to construct a prototype modulator. A 100 kW RF test facility as since been constructed which became operational in November 1972. A MIT-type klystron (VA-938D) with IKO specifications is simultaneously under test. In the following paragraphs the prototype modulator will be described. Preliminary test results will be given.

Prototype modulator

General design considerations

The klystron will only be operated at 4 discrete RF power levels, as is indicated in table 3.

Table 3: Modulator operating levels

RF peak power	1	2	4	6	MW
Cathode voltage	80	102	130	150	kV
Cathode current	44	63	91	125	A
Klystron imp.	1818	1619	1428	1200	Ω
Repetition rate	2000	1000	500	ca 80	Hz
Duty factor	10	5	2.5	0.4	%
Video peak power	3.5	6.4	11.8	18.8	MW
Transformer ratio	1:11	1:8	1:11	1:8	
Number of modules	9	15	14	22	
PFN units per mod.	1	1	2	2	
PFN-line voltage	1973	2050	2038	2046	V
Primary pulse curr.	484	504	1001	1000	A
PFN imp.	2.08	2.08	2.08	2.08	Ω
PFN rep.rate av.	512	426	398	312.5	
PFN rep.rate max.	625	625	625	312.5	
Pulse specifications:					
Flat top ripple	0.1	0.1	0.1	0.1	%
Droop of flat top	+0.5	0	-0.5		%

A high duty factor linac facility will experience a large electric power bill. In order to limit the power losses and the voltage stress of the various modulator components, a line-type modulator has to be impedance-matched to the klystron. In the design of the modulator - large effort has been spent on a further reduction - of the inherently low losses of a conventional line-type modulator. A relatively inexpensive unregulated main DC power supply will be applied to feed all 12 modulators with a single 1000 V DC buss-bar.

Much attention has also been given to the reliability of the various components since a very large number of capacitors and solid state switches, among others, will be used.

Special circuits, to be described below, were designed basically to achieve the pulse-to-pulse operation of the modulators. The complex control task for the pulse-to-pulse triggering at potentially different power levels is performed by a special digital processor.

Circuit description

The prototype modulator consist of 24 modules, each containing 2 PFN units (fig. 1 and 2). Each module feeds a primary winding of a special summing pulse transformer. By selection of the number of modules, the number of PFN units per module and the transformer step-up ratio, the video power output can be varied according to the requirements as listed in table 3. Optimum use of all the available PFN units is made by a cyclic pulsing scheme. Two spare modules have been incorporated in the design. Valuable redundancy has been obtained in this manner, since the loss of one or more PFN-units implies at most the reduction of the duty cycle and not the klystron RF peak power. The recovery time of the switching devices limits the repetition rate of line-type pulsers. High modulator repetition rate (2000 pps) has been obtained by sequentially switching low (625 Hz) repetition rate PFN units.

The schematic diagram of a PFN unit is given in fig. 3. A pulse forming network is charged to approx. 2000 V by means of a charging circuit from the external 1000 V unregulated DC power supply. Triggering of the discharge SCR's discharges the line with approx. 1000 V and 500 A into the pulse transformer.

The pulse forming network consists of two printed circuit boards, each containing 120 printed inductors and 60 capacitors (0.1 µF-2500V). Each inductor is designed (with a flat pulsetop in mind), including effects of the pulse transformer and other parasitic circuit elements. The large number of PFN units justifies this approach. Fine adjustment of the characteristic impedance will be obtained by 8 movable copper shorting vanes. The large number of pulse line sections will smooth out individual capacitor differences.

The charge circuit. The transformer step-up ratio is selected by triggering the appropriate pair of discharge SCR's. By investigating the parasitic circuit elements the rate of rise of the pulse current could be limited to 100A/µsec. Protection against forward break over and excessive reverse power is obtained by careful selection of the "snubber" circuitry. With these precautions standard unselected SCR's can be used. Such a design results in a marked reduction of RFI noise. The electrical behaviour of the special pulse transformer implies the short circuiting of all unused primaries during a discharge pulse by means of a special SCR circuit. The stored energy in the pulse transformer is transferred back into the pulse-forming network. Excess charge is dissipated in the end of line clipper.

The charge circuit is conventional. Due to the low repetition rate of each PFN unit the requirements on the charging SCR's are very moderate.

The SLS system can best be dexcribed as a non-dissipative "De Qing" circuit. The pulse-forming network is charged resonantly by means of a charging choke. Whenever the correct line voltage is obtained, Th3 is triggered, thereby transferring the stored energy of the charging choke into the SLS capacitor and back into the main DC power supply. Fine control of the RF output is obtained by small adjustments in the line voltage which are also under control of the Dig-1 processor.

Dig-1 processor (fig. 4)

The central element in this unit is a memory containing RF pulse power information for 256 pulses. This implies a minimum repetition rate of 10 Hz with a pulse-to-pulse interval of 400 µsec. The memory is loaded at present through a switch register. Eventually this will be achieved over a data line with the central control computer. The memory information is first translated into the number of PFN units to be triggered and then transferred to a (2x24 positions) shift register. By this register the individual PFN charge and dis-

charge triggers will be allocated. The out-of-order information will be stored in the control part of the processor. By means of a separate input-output unit the necessary level conversion and noise immunity is provided.

Cooling

Due to the compact construction of the modulator system the power density has increased. Consequently a special technique has been developed whereby efficient cooling has been obtained by using the liquid-vapor phase change of CCl_2F-$CClF_2$. This fluid (freon 113) is extensively used as a cleaning agent and as such is known to be inert to almost any material. Since information on the effects of prolonged contact was not available, however, this subject had to be investigated further.

Conclusion

A prototype modulator has been constructed with the afore mentioned features. Extensive testing has been started since November 1972. Each module has been tested at full peak power with 125% of the maximum design duty-factor with excellent results. The complete modulator has been tested up to 1% duty factor. Due to problems related to the klystron and the DC power supply full duty factor has not been achieved yet. The overall circuit behaviour is as expected. During the construction phase IKO decided to install only 30 of the 48 PFN units for the following reasons. The 6 MW power level has been abandoned for financial reasons and secondly a more economical version of a pulse forming network is being designed.

An elaborated measuring method is being completed capable of providing accurate pulse-flattop measurements. Pulse-to-pulse and long term stability are within 0.1%, even under extreme conditions.

The cooling system performs well. Experience obtained sofar has resulted in cooling capacities in excess of 13 W/cm^2 at an operating temperature of 48°C.

Valuable life test data could already be collected on the PFN units of full power due to the modular construction of this modulator. On the basis of these results the MTBF of the modulator is expected to be more than one year.

Because linac maintenance is planned to be excecuted during normal operation, attention has been given to limit the audic noise where ever possible.

Test results sofar have been very promising. Specifications are now being written for the final modulator series, the first of which is scheduled for operation early 1975.

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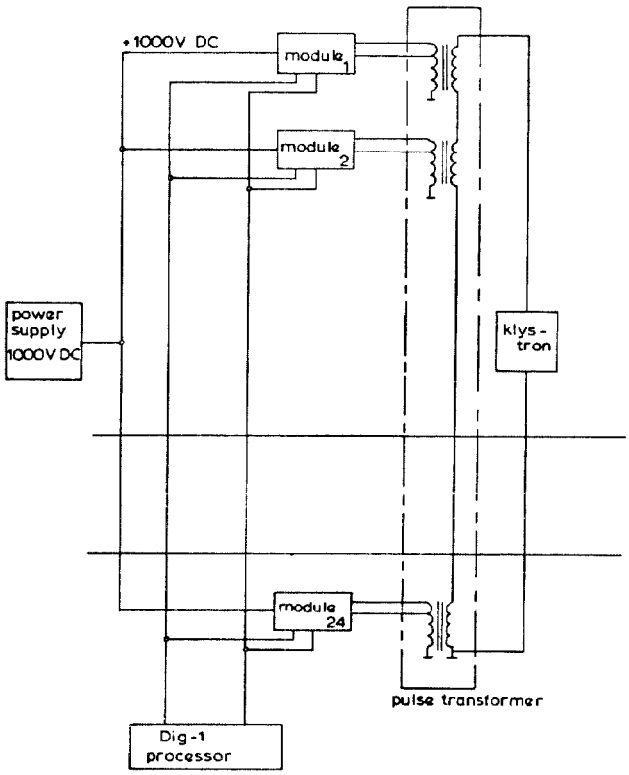

Fig. 1. Modulator schematic diagram.

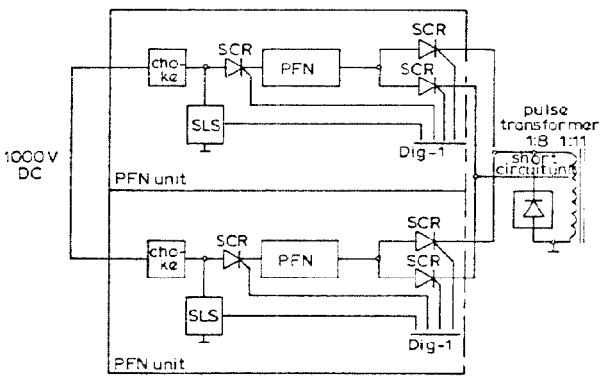

Fig. 2. Module diagram.

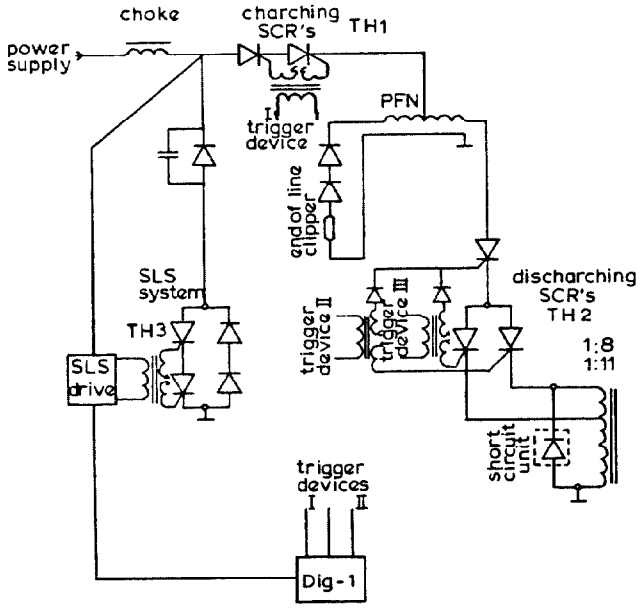

Fig. 3. PFN-unit circuit diagram.

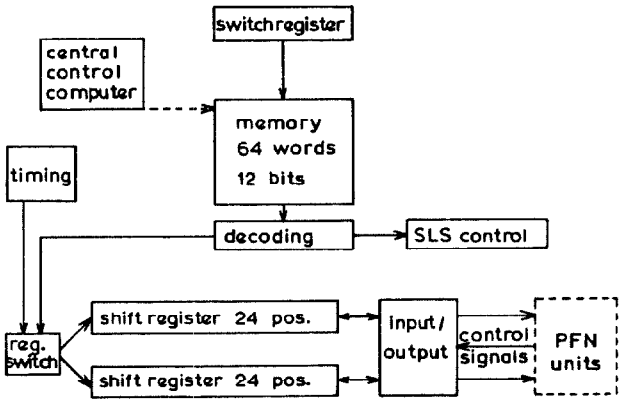

Fig. 4. Dig-1 processor.