MULTICHANNEL DOWNCONVERTER FOR THE NEXT GENERATION RF FIELD CONTROL FOR VUV- AND X-RAY FREE ELECTRON LASERS

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Abstract

For pump-probe experiments at VUV- and X-ray free-electron lasers, in the injector and bunch compression section the electron beam and timing reference must be in phase within 0.01 degree (rms) and have an amplitude stability within 10^{-4} (rms). The performance of the field detection and regulation of the acceleration RF critically influences the phase and amplitude stability. For the RF field control, a multichannel RF downconverter is used to detect the field vectors and control the vector sum of 32 cavities. In this paper a new design of an 8 channel downconverter is presented. The downconverter front-end consists of a passive RF double balanced mixer input stage, intermediate filters, and an integrated 16 Bit analog-to-digital converter (ADC). The design includes a digital motherboard for data pre-processing and communication with the controller. In addition, we characterize the downconverter performance in amplitude and phase jitter, temperature drifts, and channel cross-talk in a laboratory environment.

INTRODUCTION/MOTIVATION

In the existing low-level radio frequency system at FLASH [1], an 8 channel downconverter based on a low power Gilbert cell mixer and a 14 Bit, 1 MHz sampling ADC is used to detect the RF field of the superconducting cavitites. The intermediate frequency (IF) of 250 kHz is generated by mixing a phase modulated local oscillator (LO) with the 1.3 GHz RF from the cavity. The LO phase is switched each microsecond by 90°. This scheme needs a measurement bandwidth of > 10 MHz, due to the switching operation. It allows for detection of the in-phase (I) and quadrature (Q) values of the RF signal with a resolution of 10^{-3} in amplitude and phase. To improve the performance of the field detection, a new scheme was developed and tested.

Currently, low cost 16 Bit ADCs with sampling rates of up to 150 MHz are available with an analog input bandwidth of up to 700 MHz. This allows for the use of a higher continuose-wave IF [2] and higher sampling rates (SR) to improve the noise performance of the detector by averaging aver multiple samples and reducing the measuring bandwidth. The IQ-detection algorithm for the higher IF is based on the method of calculating Fourier coefficients [3].

A complete passive front-end is used to reduce the noise, whereas the ADC and analog front-end are integrated on one board to avoid EMI/EMC problems and the requirement of active line drivers or buffer amplifiers. A disadvantage of a passive front end is the conversion loss,

consequently a high input level is needed to operate the ADC at full scale. This leads again to errors from ADC and front-end nonlinearities. The permitted nonlinearity errors are < 1%.

DESCRIPTION OF THE FIELD DETECTOR

The field detector presented in this paper consists of a downconverter board which converts the incoming analog RF signal to a digital signal and a digital carrier board which is used for data preprocessing and communication with the controller. The scheme of the downconverter board is shown in Fig. 1.

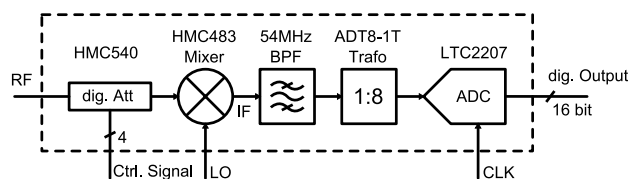The first stage of the downconverter is a digitally ad-

Figure 1: Simplified downconverter scheme

justable attenuator (HMC540[1]) which is used to set the operating point of the downconverter by changing the input signal level depending on the gradient in the cavity. The second stage is a mixer which converts the RF signal at 1.3 GHz to the IF of 54 MHz. The mixer (HMC483) is a highly linear double-balanced mixer with an internal LO buffer. The internal buffer allows for operation at a low LO power level in the range of 0 dBm. The following 3rd order integrated LC Chebychev bandpass filter[2] at 54 MHz with a bandwidth of 10% supresses unwanted mixing products. The following step up transformer ADT8-1T[3] with an impedance ratio of 1:8 provides a voltage gain of $\sqrt{8} \approx 2.8$ and converts the unipolar input to a differential output which is required for the ADC. The high-speed 16 Bit ADC (LTC2207[4]) operates at an 81 MHz sampling frequency.

To estimate the performance of the downconverter in noise and linearity, the noise figure NF_{sys} and the 3rd order input intercept point $IIP3_{sys}$ of the downconverter is calculated based on the Friis formula [4]. The parameters for each stage is shown in Tab. 1. The input attenuator

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Table 1: System parameters for each converter stage

	Att.	Mixer	BPF	Trans-former	ADC
NF [dB]	1	11	3	1	35
IIP3 [dBm]	48	36	35	35	/
G [dB]	1	−11	−3	9	/

has an insertion loss of 1 dB and is set to 0 dB attenuation. The ADC noise figure is given by the signal-to-noise ratio (SNR) of 74 dB [5]. It is valid for full-scale operation of the ADC. The overall noise figure NF_{sys} of the downconverter is 41 dB, while the system's 3rd order input intercept point, $IIP3_{sys}$, is 36.1 dBm and the system gain, G_{sys}, is −6 dB. To operate the ADC at full-scale (FS), a downconverter input power level of 17 dBm is needed. The calculated noise floor for amplitude and phase noise of −150 dBc/Hz integrated over the measuring bandwidth of 9 MHz results in a rms jitter of $0.95 \cdot 10^{-4}$. This corresponds to a SNR of −80 dB. With an intermodulation product of 3rd order, IM3, of −38.2 dBc, the amplitude error of the downconverter is given by 1.2%.

MEASUREMENT SETUP

For the laboratory characterization of the downconverter, three signals have to be generated. The RF input signal at 1.3 GHz with an adjustable signal level, the LO signal for the mixer at 1.354 GHz with 0 dBm, and the sample clock (CLK) for the ADC at 81 MHz with approximately 10 dBm. The setup for generating these test signals is depicted in Fig.2.
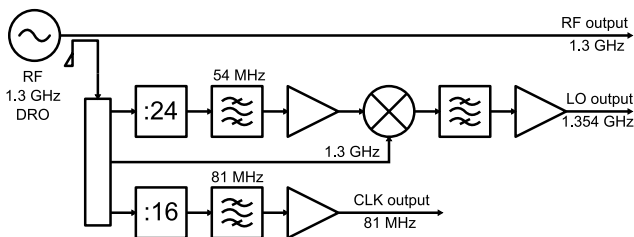

Figure 2: Signal Generation Setup

This signal generation setup is chosen to assure correlated phase noise on all three input signals, except for noise from the amplifier and frequency divider. Otherwise, the uncorrelated phase noise limits the resolution of the measurement.

A 1.3 GHz Dielectric Resonator Oscillator (DRO) is used as RF input and as the reference for the LO and CLK generation. The LO is generated by dividing the 1.3 GHz by 24 and mixing it with the 1.3 GHz again, while the CLK is generated by dividing the 1.3 GHz by 16. Amplifiers, attenuators, and filters are used to adjust signal levels and supress unwanted frequencies.

The measurement setup to characterize the downconverter

is shown in Fig. 3. The signal generation setup is connected to the downconverter (DUT). For linearity characterization, a second signal source (RF 2) with a frequency shift of 1 MHz is added. The amplifiers in front of the combiner are used for signal sources decoupling.

For drift characterization, the converter and the signal generation setup are installed separately in an oven with a temperature stabilization of about $0.1\,°C$. To determine the temperature coefficient of the downconverter the response of a temperature step of approximately $10\,°C$ on oven No.2 is measured. A rough temperature measurement is done to estimate the influence of each converter stage on the temperature coefficient of the system.

A logic analyzer is connected to the DUT, (ADC) to acquire and analyze the digital data. For temperature recording, a conventional data logger is applied.
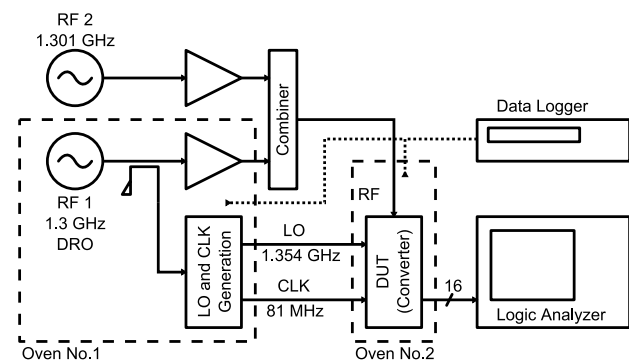

Figure 3: Measurement setup for downconverter characterization;

MEASUREMENT RESULTS

The measured rms amplitude and phase jitter are shown in Fig.4. The measured values are $0.8 \cdot 10^{-4}$ for amplitude and $0.9 \cdot 10^{-4}$ rad for phase jitter within a measurement bandwidth of 9 MHz. The phase jitter corresponds to an integrated timing jitter of 18 fs at 1.3 GHz. For a measuring bandwidth of 1 MHz, the rms jitter can be reduced to $0.3 \cdot 10^{-4}$ in amplitude and $0.3 \cdot 10^{-4}$ rad in phase, corresponding to an rms timing jitter of 6 fs at 1.3 GHz.

A measured system IIP3 of 33.8 dBm is comparable to the calculated one and corresponds to an IM3 level of −33.6 dBc at an input power level of 17 dBm. The main contribution is caused by the mixer due to the high input power level. The requirement that non-linearitiy errors are smaller than 1 % leads to an IM3 level of −40 dBc.

The channel-to-channel crosstalk is determined to be −66 dB by measuring two channels in parallel, one with input power, while the other one is terminated with 50 Ω at the input. Its main contribution is caused by the low RF-to-LO isolation of the mixer and the power splitter in the LO distribution.

The results of the drift characterization are shown in Fig.5. The temperature coefficient of the downconverter for am-
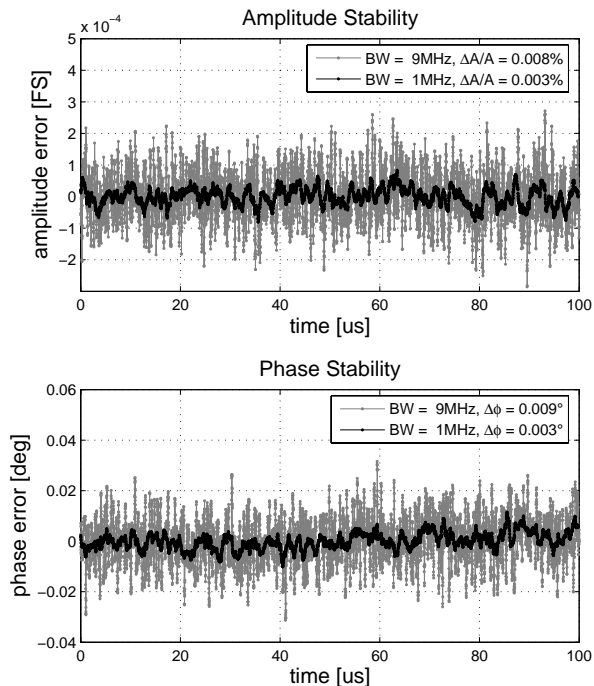
Amplitude Stability

Phase Stability

Figure 4: Amplitude and phase stability of a single down-converter channel

Amplitude and Phase Drift

Temperature Profile

Figure 5: Results of the drift measurement with a temperature step of $12°C$.

plitude and phase are $\theta_A = 2 \cdot 10^{-3}/°C$ and $\theta_\phi = 0.2°/°C$. The main contribution to θ_A is caused by the digital input attenuator, while the contribution of θ_ϕ is given by the mixer and the bandpass filter. The temperature-sensitivity of the ADC is insignificant for amplitude and phase stability.

SUMMARY AND OUTLOOK

A multichannel downconverter using a CW IF modulation scheme is presented. For a measurement bandwidth of 9 MHz, an rms amplitude stability of $0.9 \cdot 10^{-4}$ and an rms phase jitter of $0.9 \cdot 10^{-4}$ rad are achieved. Jitter and drift of the LO directly limits the detector performance, whereas the ADC clock jitter is less significant. The downconverter nonlinearity of about -33.6 dBc nearly fulfills the requirement. Its temperature coefficients for amplitude and phase are $\theta_A = 2 \cdot 10^{-3}/°C$ and $\theta_\phi = 0.2°/°C$, requiring drift compensation. Beside using a passive low-noise front-end the improved detection resolution is caused by the detection scheme and by averaging. Presently, the ADC limits the noise performance of the field detection. To improve the downconverter linearity linearization techniques using a calibration signal have to be applied.

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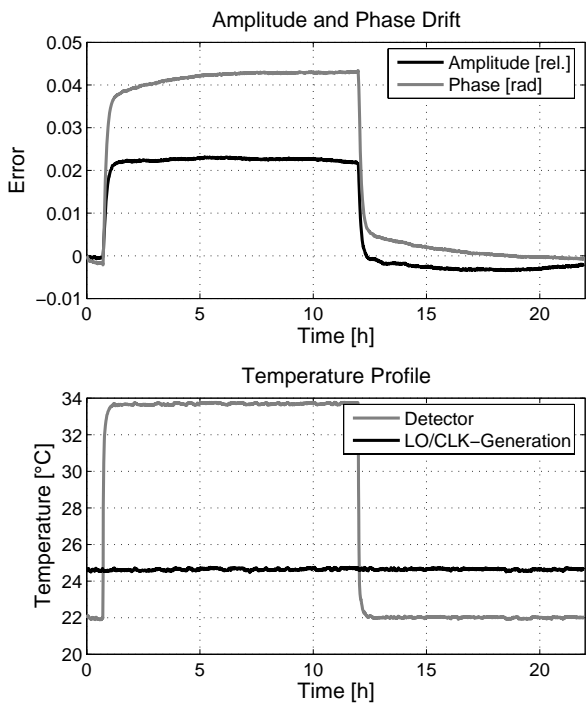[5] W. Kester, "Analog-Digital Conversion", Analog Devices, 2004