OPERATIONAL EXPERIENCE WITH THE SPALLATION NEUTRON SOURCE HIGH POWER PROTECTION MODULE *

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Abstract

The Spallation Neutron Source (SNS) High Power Protection Module provides protection for the High Power RF Klystron and Distribution System and interfaces with the Low-Level Radio-Frequency (LLRF) Field Control Module (FCM). The fault detection logic is implemented in a single FPGA allowing modifications and upgrades to the logic as we gain operational experience with the RF LINAC systems. This paper describes the integration and upgrade issues we have encountered during the initial operations of the SNS systems.

INTRODUCTION

The SNS LLRF Control System is comprised of three main components; the Field Control Module (FCM), High Power Protection Module (HPM), and the reference system. The High Power Protection Module detects faults in the High-Power Distribution System and interfaces with the Field Control Module (FCM) and the Machine-Protection System (MPS) to provide rapid shutdown of the RF drive. For fault detection, the HPM monitors up to seven (7) RF channels, fourteen (14) fiber optic arc detector channels (FOARC), a hardware interface channel, and several "soft" EPICS (Experimental Physics and Industrial Control System) based channels. It provides a central point for various systems like vacuum, cryogenics, and water (RCCS) to interface with the RF control system.

Figure 1: High Power Protection Module

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ARCHITECTURE

The HPM design is based on a single Field Programmable Gate Array (FPGA) utilizing an Altera 10K family device. A simplified block diagram is shown in figure 3 for reference. The module can be broken down into three major sections. The first is the RF channel fault detection state machine, second is the FOARC detection logic, and the third is the VXIbus interface. The VXIbus interface was designed at LANL and is a proven design utilized on several modules. It provides the interface between the logic of the HPM and the VXI backplane. All user interaction with the system is done through EPICS via the Input/Output Controller (IOC), backplane, and this interface.

RF Detection

The module can monitor up to seven RF channels. The RF signals are detected using Analog Devices AD8313 logarithmic detector. This broadband RF detector is capable of detecting RF signals from 100 MHz to 2.5 GHz with a 70 dB dynamic range. The HPM is calibrated for use from +10 dBm to -40 dBm. A 15 dB attenuator is installed at the input of the detector; this places the input signal in the linear range of the part. Figure 2 shows a typical response with all seven RF channels plotted.

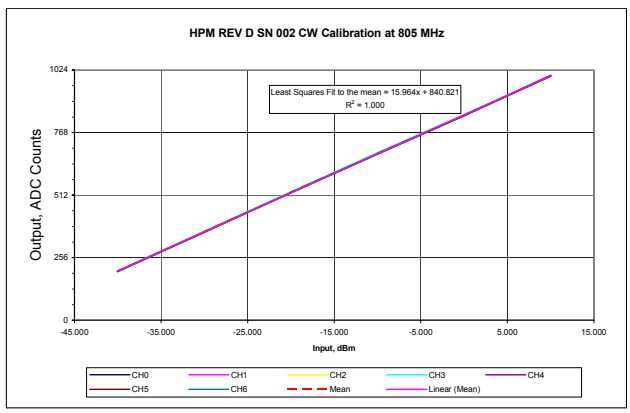

Figure 2: RF Channels 0-6, after calibration

The RF inputs are conditioned prior to being digitized by 10 bit parallel ADCs. The data from all analog channels are latched to provide synchronous sampling of all channels. The FPGA controls the digitizing process and data management; each channel is updated every 2uS. Theoretically, given a 10-bit ADC and an accuracy specified at +/- 2 counts, +/- 0.1dBm should be able to be measured. Operational experience with the module has

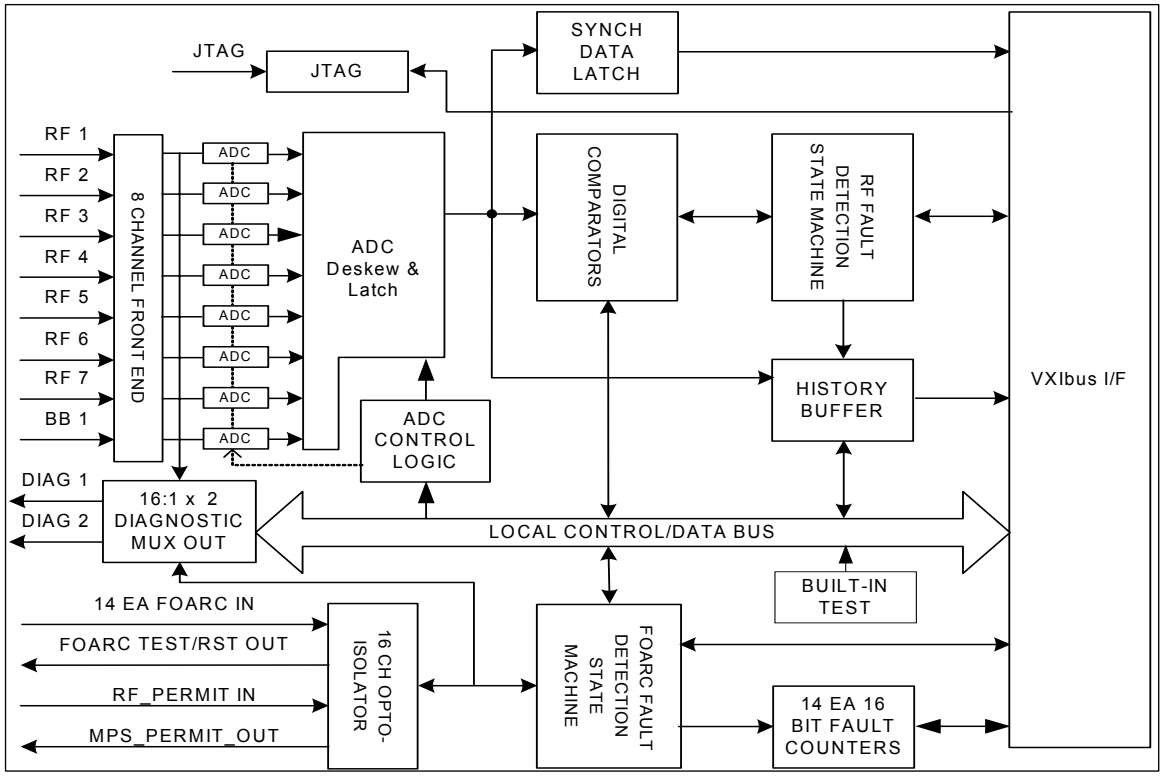

Figure 3: HPM Top-Level Block Diagram

shown that +/- 0.25 dBm is closer to the normal error in measurement. This seems to be attributed to the background noise in the klystron gallery. In addition to the seven RF channels, a baseband input channel is available.

The RF signals are monitored by the various channels and if the signal is above a user defined threshold action is taken to protect the system. Cavity fill time delay and fault persistence are used to minimize nuisance trips. Fill time delay is used to ignore RF trips during the period of time the cavity is filling. This eliminates the problems of forward and reflected power overshoot during turn on. With the normal-conducting cavities, fill time delay is set fairly short, averaging 25uS in duration. With the superconducting cavities, fill time delay is set much longer, averaging 300 uS in duration. Fault persistence uses a duration timer set by the user. The timer sets a minimum period that the fault must persist for before a fault is declared.

The response time from detecting a RF fault until the RF drive is inhibited averages less than 100 nS. This includes the time needed to remove the permissive to the machine protection system (MPS) to inhibit beam. Figure 4 shows an average response to a RF fault, the top trace shows the RF permit being removed and the bottom is the MPS signal out.

Fiber-Optic Arc Detection

The HPM has fourteen FOARC inputs that are opto-isolated at the HPM to avoid ground-loops and noise from the Advanced Ferrite Technologies (AFT) fiber-optic arc-detection chassis. This chassis detects the actual waveguide arc and sends a fault signal called an FOARC to the HPM for Processing.

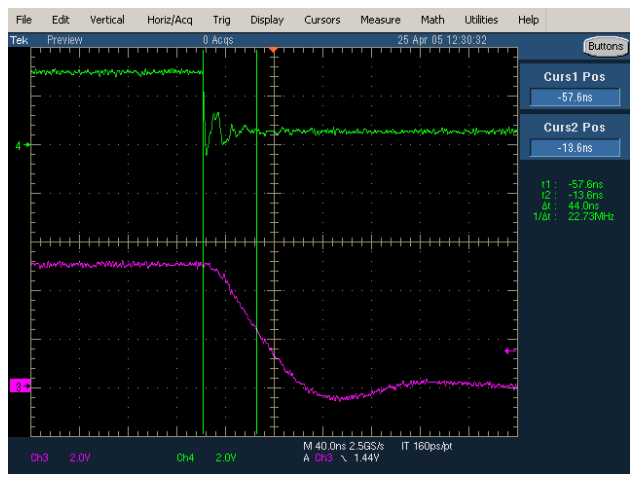

Figure 4: RF Fault Response

When an FOARC is detected, the HPM turns off the RF signal and drops the MPS permit until the end of the RF pulse or until the fault clears, whichever is longer. The fill time delay used for the RF channels does not affect the FOARC channels and faults are monitored for the entire pulse. Figure 5 shows a typical response time to inhibit the RF drive and pull the MPS permit; an average response time is 160 nS. The HPM provides an EPICS activated built in test function for the AFT fiber-optic arc-detection chassis. The test signal will fault all FOARC

channels and provide a reset signal to the chassis after the test to restore normal operation.

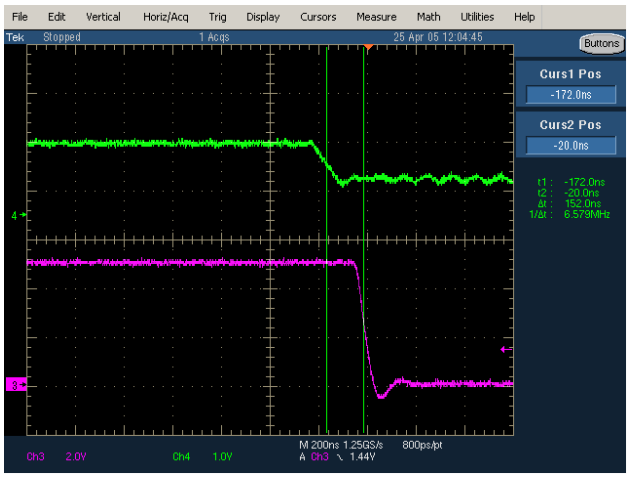

Figure 5: FOARC Response

Additional Features

The HPM has two diagnostic multiplexers to allow monitoring of the data prior to digitization and can be used for all inputs. They consist of a pair of single pin LEMO 50 ohm connectors on the front panel of the HPM. These EPICS selectable monitor ports can provide access to all ADC channels, the TTL backplane signals, and all FOARC channels for monitoring up to two channels simultaneously. History buffers are provided and function similarly to a dual channel digital oscilloscope. Figure 6 shows the EPICS interface to the history buffers. This allows the user to quickly check signals on the board including signals inside the FPGA that would not be normally available.

IMPROVEMENTS

Originally, fault counters were only available for the FOARC channels but have been added to all channels to provide an easy way to determine which channel is faulting regularly. These counters are archived so that statistics can be compiled on individual cavities. A flag is sent to EPICS when bit 15 of the counter is set to request a reset prior to overflow.

In the SCL section of the LINAC, most VXI crates support two LLRF systems. The ability to individually set the timing pulse width and rep-rate per system was not available due to a shared backplane. A local bus has been added to solve this problem and timing is now provided to each FCM/HPM pair. This local bus is also used to provide a redundant shutdown signal and is planned to be modified in the future to include the beam permit signal.

Some additional improvements have been made to the fault detection logic to lessen nuisance trips. Detection of faults has also been limited to the duration of the RF pulse so that noise associated with data transfer across the backplane does not cause false trips. As we continue to gain operational experience with the HPM additional improvement will be made to support changing operational needs.

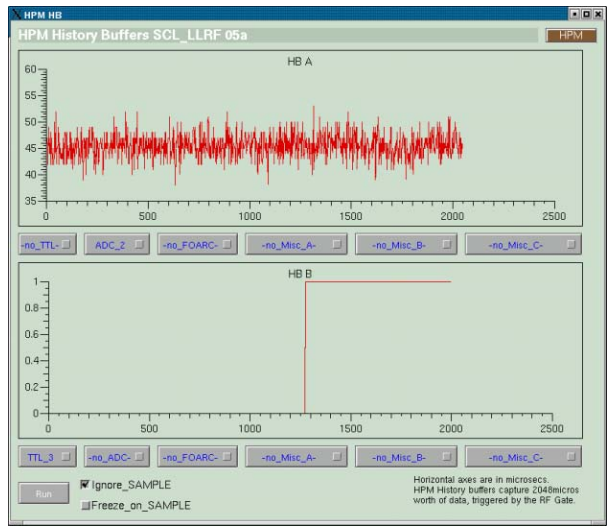

Figure 6: History Buffer EPICS Interface Screen

SUMMARY

The testing and commissioning of the normal conducting LINAC is completed and the HPM has proven to be a reliable design. The AHDL code has seen several revisions to support changes needed to meet operational needs. With the current version of the firmware, only 37 percent of the capabilities of the FPGA are utilized, leaving room for additional growth as we commission the superconducting portion of the LINAC.

ACKNOWLEDGEMENTS

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