ENHANCEMENTS FOR THE 1 MW HIGH VOLTAGE CONVERTER MODULATOR SYSTEMS AT THE SNS*

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Abstract

The first-generation high frequency switching megawatt-class High Voltage Converter Modulators (HVCM) developed by Los Alamos National Laboratory for the Spallation Neutron Source (SNS) at Oak Ridge National Laboratory have been installed and are now operational. Each unit is capable of delivering pulses up to 11 MW peak, 1 MW average power at voltages up to 140 kV to drive klystron(s) rated up to 5 MW. To date, three variations of the basic design have been installed, each optimized to deliver power to a specific klystron load configuration. Design improvements, with the primary intention of improving system reliability and availability, have been under development since the initial installation of the HVCM units. This paper will examine HVCM reliability studies, reliability operational data, and modifications and improvements performed to increase the overall system availability. We will also discuss system enhancements aimed at improving the ease of operation and providing for additional equipment protection features.

HARDWARE OVERVIEW

The HVCM system block diagram is shown in Figure 1 below along with photographs of the major pieces of equipment. Each HVCM derives it bus voltage from a substation cast-coil 13.8 kV to 2100 V ΔY transformer rated at 1.5 MVA. To minimize harmonics returned to the point of common coupling, 5th and 7th harmonic traps are incorporated in the transformer enclosure. Each transformer is followed by an SCR regulator which provides voltage regulation over a wide range of loading configurations as well as providing a soft-start function. Primary energy storage for the modulator is accomplished at ±1200 V utilizing specially developed low inductance self-clearing metallized hazy polypropylene capacitors. These capacitors fail with a gradual degradation of capacitance, do not fail short, and have a history of 300,000 hours lifetime in traction motor applications overseas.

Three IGBT H-brides switching networks are used to generate bipolar 20 kHz drive currents to a transformer primary. The IGBTs are driven for the duration of the klystron cathode pulse required. The nanocrystalline boost transformers are wound with a turns ratio of up to 19:1 to realize voltage gain on the secondary. However, due to the resonant nature of the secondary circuitry, gains of up to 60:1 are achieved by designing the transformers for a desired leakage inductance. The resonant nature can also achieve turn-on zero-voltage-

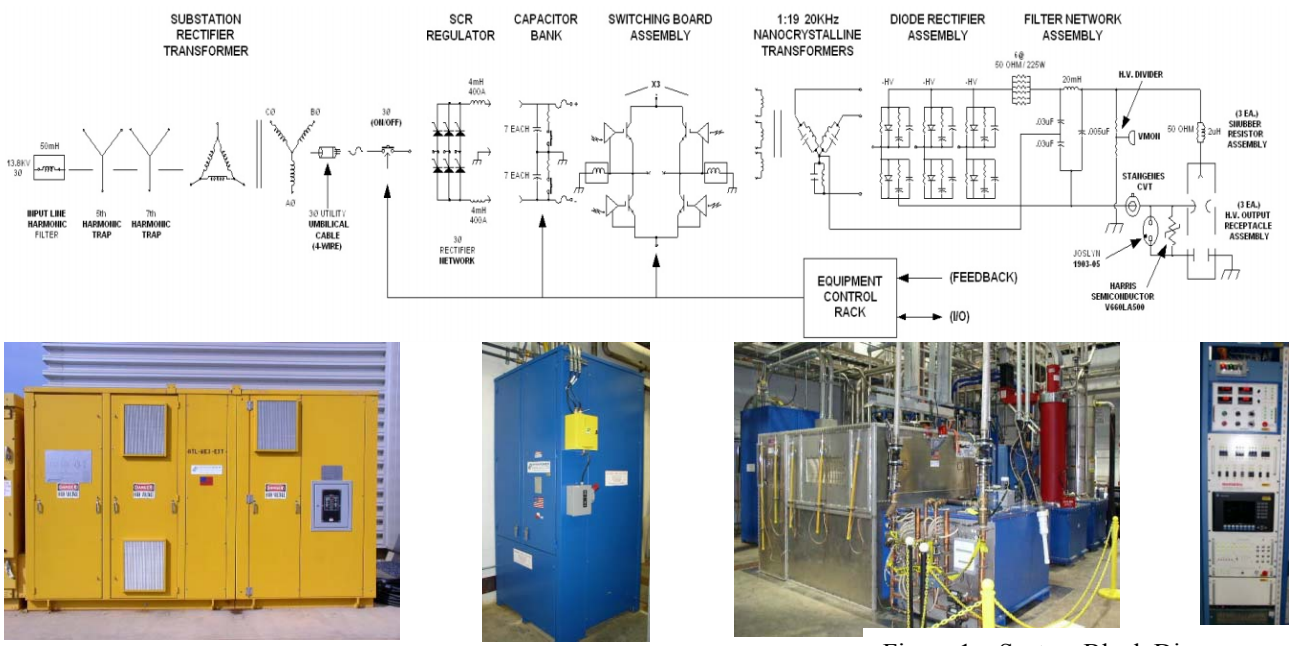

Figure 1 – System Block Diagram

* SNS is managed by UT-Battelle, LLC, under contract DE-AC05-00OR22725 for the U.S. Department of Energy. SNS is a partnership of six national laboratories: Argonne, Brookhaven, Jefferson, Lawrence Berkeley, Los Alamos and Oak Ridge.

switching, reducing IGBT switching losses. An optimized tune will also reduce turn-off commutation currents, reducing the diode losses in the opposite (complementary) IGBT module. Turn-on is also soft with minimal forced commutation of the body diode on the IGBT module.

Resonant rectification techniques are achieved by placing discrete capacitors across the groups of rectification diodes. These capacitors, combined with the transformer secondary shunt peaking capacitor, achieve the 20 kHz resonance desired. The rectification capacitors also bypass the diode switching transients and overshadowing the "Miller" capacitance of the diodes, thereby providing more uniform voltage distribution across the diodes. A traditional "Pi-R" filter network is employed on the output, with the filter capacitance chosen to provide adequate filtration without excess stored energy.

RELIABILITY STUDIES

Early on in the design program, an analysis was performed to predict the Mean Time Between Failure (MTBF) of the HVCM systems based on MIL HDBK 217F. While admittedly not well suited for predicting failures in pulsed systems, it was useful for predicting relative failure rates and developing mitigation to improve those subsystems with anticipated poor rates. Initial predictions of MTBF for the system were 3480 hours before any maintenance schedules or mitigation factors were applied, with the largest contributor to the failure rate being the SCR Controller. After adjusting component MTBF rates for scheduled maintenance and implementing standard techniques for improving poor failure rate components, the anticipated system MTBF is now about 20,000 hours. While still short of the goal of 24,800 hours necessary to meet equipment availability goals, it is only an estimate and the real statistics must be borne out in the operational performance of the HVCM.

Operational History

The first modulator was installed and operational by December of 2002, and as of April 2005, all 15 modulators have been installed. Initial operation was performed at 1 Hz to support front end testing, with only the RFQ klystron producing RF. Since that time, operation to 60 Hz with a full klystron load has occurred, although present operations are limited to 30 Hz. Table 1 summarizes operational history for the various sections of the linac.

Since initial operation of the first modulator, we have had 3 failures of the HVCM system and 7 failures of the SCR Controller at Oak Ridge National Laboratory (ORNL). The first HVCM problem was a catastrophic failure of the potted secondary winding on one of the boost transformers due to corona in trapped air bubbles. We immediately abandoned that design for an open-winding configuration and have not had any problems since. The other two failures were with the IGBT switch plate assembly. In one case, poor mounting and torquing techniques led to hot spots on the module. The cause of the other failure was never determined with any degree of certainty. SCR failures were due to a variety of quality assurance and design shortcomings, which will be discussed later in this paper.

Table 1 – HVCM Operational History

SYSTEM	***OPERATIONAL HOURS***
DTL modulators	
low average power (<5 Hz, single klystron)	**1500**
full average power operation	**1780**
Dual/triple klystron to 30 Hz, peak power	**9063**
CCL modulators (peak power, ≤30 Hz)	**7763**
SCL modulators (peak power, ≤30 Hz)	**1470**
RFTF-ME (1 klystron to full duty)	**1000**
LANL unit full average power	**2000**
TOTAL	**24,576 hours**

HVCM UPGRADES

While most of the failures experienced at ORNL are attributed to workmanship issues, our operational experiences have led to a better understanding of the dynamic performance of the HVCM. Techniques to improve the performance areas of concern will be further investigated.

Concerns over evidence of extreme temperatures on the boost transformer winding spacers, coupled with oil flow measurements at ORNL, led us to redesign the plumbing system inside the oil tank. The transformers are located at one end of the tank, opposite of the heat exchanger and pump. We decided to force all pumped oil to the transformers and rely on natural convection for cooling of other components. This accomplishes forced convection cooling of the major heat source inside the tank as well as sets up a circular circulation path for oil inside the tank. Since performing this modification, we have had no transformer failures.

Measurements of the IGBT over current response time, which relies on Rogowski probes placed between the collector and emitter of the devices, indicate the fault condition would have to exist for several microseconds before the control chassis would disable the gate drives. In a shoot-thru fault condition, this delay would likely result in destruction of the IGBTs. While still in the prototype stages, we have developed an anti-saturation network on the IGBT gate drive cards which continually monitors V_{CE} across all IGBTs and responds in less than a microsecond to any fault condtions.

A redesign of the output choke mechanical structure was necessitated due to the tremendous amount of audible noise generated by this device and the concern over work hardening of materials, shifting conductors with resultant arcing, etc. An improved core clamping design resulted in a reduction of the noise by a factor of 2.4. A redesign of the winding using stiffer conductor and higher winding tension is also under investigation.

A Dynamic Fault Detection Chassis has been designed to detect abnormal changes in the output voltage during the output pulse arising from arcing of the transformer secondary windings or other anomalies. It will also incorporate core flux monitors and diagnostics to automatically shut the system down in the event of a fault.

SCR Controller Upgrades

The majority of the SCR upgrades are predicated on the poor MTBF rate of this subsystem. Analysis of the failed SCR wafers by the manufacturer has shed some insight into the problems. Figure 2 is a sampling of failed wafers indicating dv/dt (edge destruction) and di/dt (gate-cathode interface holes) failures.

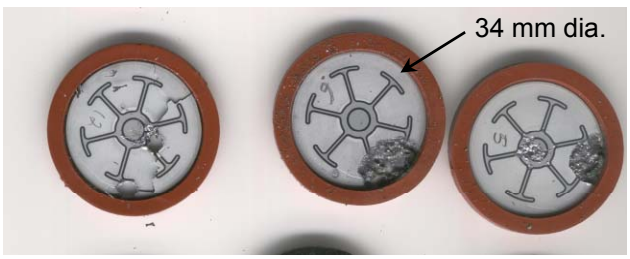

Figure 2 – SCR Wafers Showing Damage from Failure

dv/dt failures are likely due to inadequate snubbing of the transients generated at the onset of device commutation. The originally-installed snubber resistors were wire-wound devices with a series inductance of 26 µH, according to the manufacturer. This undesired inductance in the snubber circuit limits the response time and has been upgraded with non-inductive resistors.

di/dt failures are likely the result of spurious gate firing signals or insufficient gate drive. The original design utilized switching on the cathode side of the drive as well as lower than recommended drive levels. Also, due to circuit layout, noise immunity was poor. We have since corrected those issues with a new driver card which incorporates fiber optic decoupling, gate referenced switching, higher drive levels, and a negative gate bias during the off-state. Although operational hours are low with this redesign, to date no failures have occurred since incorporating this modification.

To attempt to minimize SCR damage and switchgear failures during faults, we have been attempting to provide better coordination between the 13.8 kV switchgear fuses and the SCR fuses. We have also incorporated circuitry which opens the 2100 V contactor in about 13 ms, considerably faster than the 60-70 ms it took previously.

SCL HVCM 60HZ OPERATION

Project schedule constraints did not allow testing of the SCL HVCM prior to installation. Initial attempts at 60 Hz full average power operation of the SCL modulators proved unsuccessful. After only seconds of operation, the A phase IGBTs failed catastrophically due to transient heating superimposed on the steady-state heating of the IGBT and/or body diode dies. Figure 3 shows the current waveforms associated with the A phase complimentary pair IGBTs. Note the commutation current of approximately 1500 A and the body diode forward current of approximately 650 A.

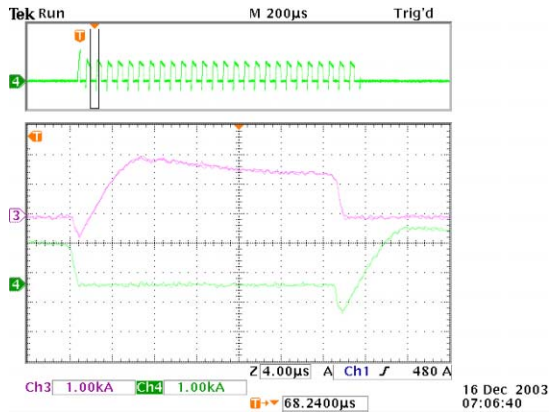

Figure 3 – IGBT Currents for 69 kV Operation, Initial Tune, both H-bridge IGBT currents shown

After comparison with the normal conducting linac modulators, it was determined that the secondary resonant circuit needed to be changed to provide the proper load impedance match. This was accomplished by reducing the number of secondary winding turns and increasing the shunt peaking capacitance across the transformer, thereby changing the resonant frequency of the secondary. The new results are shown in Figure 4, with a significant reduction of diode peak and commutation current levels at the expense of a higher peak IGBT current. Successful operation at 60 Hz has now been demonstrated with this modification

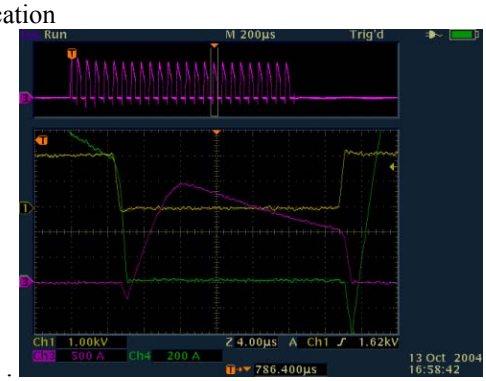

Figure 4 – IGBT Currents for 69 kV Operation, Final Tune, I_C (magenta) and V_{CE} (yellow) shown