BEAM TESTS OF A NEW DIGITAL BEAM CONTROL SYSTEM FOR THE CERN LEIR ACCELERATOR

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Abstract

The Low Energy Ion Ring (LEIR) is a major component in the Large Hadron Collider ion injector chain. We have been developing an all-digital beam control and cavity servo system for the RF acceleration in LEIR. The system is housed by VME motherboards that may hold various daughter boards. Fast tasks are executed in Field Programmable Gate Arrays (FPGAs), slower tasks and communication with the software layer above are achieved in Digital Signal Processors (DSPs).

We describe a simplified system prototype, which we tested with low intensity beams on the CERN PS Booster (PSB). The aim was to verify the combined DSP+FPGA architecture and the feedback loop dynamics. An additional goal was to deploy and validate novel software concepts, such as reference-functions and timings generation, and user-selectable digital data acquisition.

INTRODUCTION

A new all-digital beam control and cavity servoing system is under development for CERN's LEIR [1,2]. During the PSB 2004 run we performed beam tests of a prototype [3] of the LEIR system, extending previous tests [4]. Operation with phase loop, radial loop, radial steering and frequency program was achieved; the beam was successfully captured, steered and accelerated.

PSB and LEIR, with their rather high revolution frequency f_{REV} and synchrotron frequency f_S, are the most challenging CERN machines in terms of required bandwidth for the beam phase loop. Beam testing in the PSB is convenient as fully parasitic tests may be run if only a low intensity is needed. The PSB is also an attractive benchmark since its f_S and f_{REV} are comparable to LEIR's design values. The LEIR cycle lasts 3.6 seconds [1]; the design f_{REV} range is 0.361 MHz (injection) to 1.423 MHz (extraction), the whole acceleration phase taking about 1 s. The expected f_S range is 600 Hz to 2 kHz. In the 1.2 s PSB proton beam cycle [5] the acceleration phase takes about 0.5 s and f_{REV} values range between 0.599 MHz and 1.7458 MHz. The actual f_S ranges between 2 kHz (injection) and 470 Hz (extraction). The time from each cycle start is known as ctime; injection occurs at 275 ms and extraction at 810 ms.

SYSTEM OVERVIEW

Figure 1 outlines the system prototype (dashed box) for the PSB tests [3]. It includes a DSP carrier board hosting three daughter boards: **a)** a Digital Down Converter (DDC), performing digitisation, digital low-pass filtering and decimation of analogue signals; **b)** a Master Direct Digital Synthesiser (MDDS), generating an RF analogue clock (MDDSC) signal from a 100-MHz clock reference; **c)** a Slave Direct Digital Synthesiser (SDDS) generating a RF analogue signal from the MDDSC.

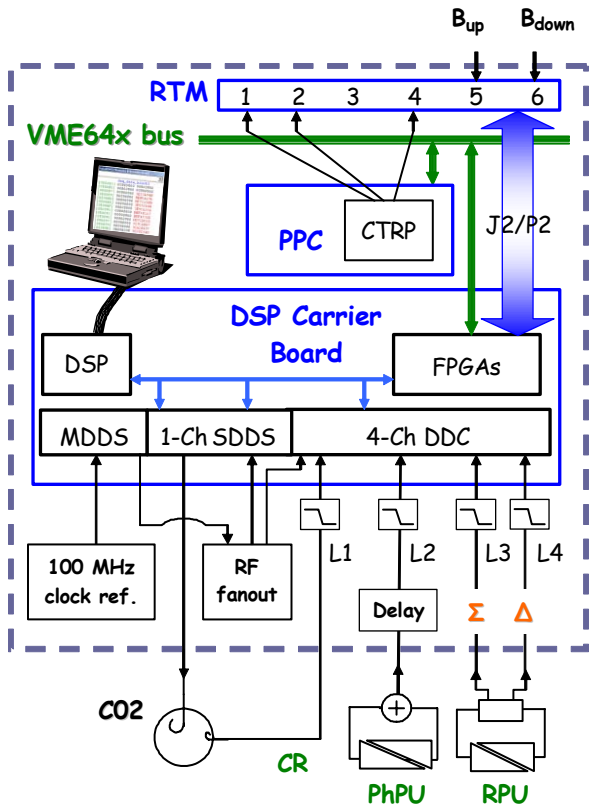

Figure 1: The prototype used for the PSB tests.

The MDDSC is fed to the DDC and SDDS via a standard RF fanout module. Its frequency f_{MDDS} is 16 times the f_{REV} calculated by the DSP. The SDDS generates the cavity modulation voltage as $f_{MDDS}/16$. The PSB standard hardware controls the cavity voltage envelope.

A Rear Transition Module (RTM) allows additional analogue inputs to be sent to the FPGAs on the DSP carrier board via the VME64x J2/P2 connector. The signals B_{up} and B_{down} derived from the bending field, are used to implement a B-train counter. A timing receiver module (CTRP), hosted by the PowerPC (PPC) VME board, generates machine-related timings and the fixed-frequency DSP sample clock (DSPSC). These are fed to the DSP carrier board via the RTM. The DDC daughter board receives signals from the phase pick-up (PhPU), the C02 cavity return (CR) and the radial pick-up (RPU) after low-pass filtering via filters L1 to L4. The DDC digitises

their signals with a sampling frequency set to f_{MDDS}, then down converts, filters and passes them to the DSP. A 310 ns analogue delay is applied to the PhPU signal to equalise the group delays in the PhPU and the CR paths. The phase and radial loop sampling frequencies are 90 kHz and 12.7 kHz, respectively. The phase loop is AC-coupled, with a cut-off at 10 Hz to reduce static frequency errors associated with a DC-coupled phase loop. A laptop runs the DSP and uploads the code to FPGAs and DSP.

HARDWARE

The DSP carrier board [6] is a 6U VME board with a 32-bit slave interface. It hosts four FPGAs, one ADSP21160 DSP and two memory blocks. The daughter boards are based on Altera FPGAs. The MDDSC runs at up to 35 MHz. The MDDS uses an Analogue Devices' AD9754 digital/analogue converter, a 14-bit resolution device capable of generating outputs with update rates of up to 125 MHz. The SDDS daughter board is similar to the MDDS daughter board, apart from the output antialiasing filter. The four-channel DDC daughter board carries four 14 bit, 80 MHz Analog Devices AD9245 analogue/digital converters, clocked by the MDDSC. L1 to L4 are antialiasing filters. The C02 cavity works in the frequency range 0.6 - 1.8 MHz thus allowing operating at the RF harmonic h=1 [5]. The RPU is based on metallised ceramic tubes with sandblasting-formed electrodes. It is provided with a sum (Σ) and four difference (Δ) electrodes. The PhPU is described elsewhere [7,8].

SOFTWARE

FPGA

The FPGA code deployed for the DSP carrier board implements the board VME interface and address decoding, a B_{up}/B_{down} counter and a DSPSC counter. It also generates an interrupt on the DSP. The DDC FPGA code implements a programmable DDC, which includes a decimating Cascaded-Integrator-Comb (CIC) filter. By developing the DDC in FPGA the group delay is minimised, an important feature in a feedback loop. The CIC parameters are set to different values depending on the channel and on its use. The same FPGA code for the MDDS and SDDS implements a digital synthesiser.

DSP

The DSP code performs three tasks, executed as interrupt service routines. The slow-loop task carries out background jobs, such as cycle-start DSP initialisation and DSP data refresh. The internal DSP timer triggers it every T_{SL} = 1 ms. The fast-loop task is responsible for core activities such as phase and radial loops, radial steering, frequency program execution and f_{MDDS} updating. The DSPSC triggers it every T_{FL} = 11.1 μs. The external timing task initialises several parameters and starts the DSP beam control for the next cycle. It is triggered by the start cycle RTM timing input.

The DSP implements a novel approach [3] to the generation of vector based reference-functions and timings, indicated here as soft-GFAS and soft-timings, respectively. These are functions traditionally generated by VME hardware as analogue output. We also developed DSP-Oasis, a user-selectable digital data acquisition function providing diagnostic and troubleshoot access points to check real-time data and to save them for later analysis.

The system prototype implements frequency program, radial steering, phase and radial loops capabilities. In the frequency program, the injection frequency is user-selected to optimise the capture process. After a soft-timing, the frequency program shifts to using the B_{up} and B_{down} values. The radial steering is implemented via a soft-GFAS. The phase loop, closed by a soft-timing, is AC-coupled via a low-pass, first order IIR filter. The radial loop, closed by a soft-timing, uses a Proportional-Integral regulator (PI) allowing two different settings in one cycle.

BEAM CONTROL TESTS

The beam controlled with the system prototype was injected and accelerated in PSB ring four with the PSB ejection kicker disabled; the beam was not extracted. The beam was kept at low intensity, typically about 10^{11} protons, to avoid triggering the beam loss monitor alarm. On a few occasions, a higher intensity (~ 10^{12} protons) was allowed. The phase loop was closed at ctime = 275.3 ms and the radial loop at ctime = 282 ms. In the phase loop tests the radial loop was not closed.

Capture and Acceleration Efficiencies

The capture and acceleration efficiencies were measured by continuously controlling one user beam and taking snapshots of the operational display. The beam intensity was varied from one cycle to another and the captured particles number range was 1.4 10^{11} to 1.8 10^{12}. Measured efficiencies were between 95% and 100%, similar to analogue PSB beam control efficiencies.

Phase Loop Dynamics

In the Phase Loop Dynamics tests, we added a 0.2 rad step-function stimulus to the measured phase error ϕ_m, starting at ctime = 285 ms. This modified ϕ_m was fed to the phase loop and the response was observed by the DSP-Oasis measurement. The radial loop was kept open.

The nominal phase loop bandwidth was 7 kHz. The high and low frequency poles f_H and f_L of the closed loop system with the phase loop active were calculated to be 7 kHz and 570 Hz, corresponding to time constants τ_{HPL} = 23 μs and τ_{LPL} = 280 μs. Figure 2 shows the measured phase error ϕ_m versus ctime and the lower plot highlights the fast time constant of the decaying part of the curve. It was obtained by setting the DSP-Oasis sampling period t_{DAQ} to T_{FL}. The measured fast time constant was ~25 μs. The upper curve has a slow time constant of ~300 μs, obtained with $t_{DAQ} = 5 \cdot T_{FL}$. Both time constants agree with the expected values of τ_{LPL} and τ_{HPL}.

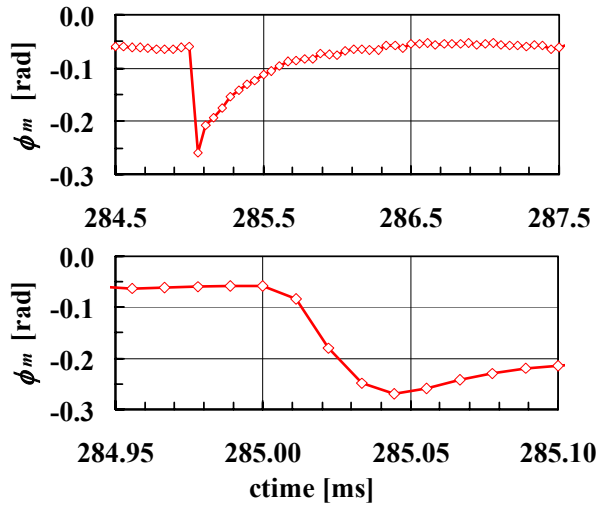

Figure 2: Plots of the phase error ϕ_m versus ctime.

Radial Loop Dynamics

For the Radial Loop Dynamics tests the two PI settings were optimised for ctime = 467 ms and for ctime = 612 ms. This was achieved by setting the PI regulator zero so as to cancel the phase loop low frequency pole f_L, at those ctimes. The PI radial loop gains were chosen such that the dominant radial closed loop time constant τ_r is 2 ms.

The beam radial position was varied by means of a radial steering reference function with two 5 mm steps: one at ctime = 467 ms and another at ctime = 617 ms. Figure 3 shows the radial position r, acquired by DSP-Oasis as a function of ctime. The lower plot zooms the upper one on the ctime corresponding to the steep radial position first change. For both plots we set $t_{DAQ} = 48 \cdot T_{FL}$. As expected, the radial response time constant was 2 ms.

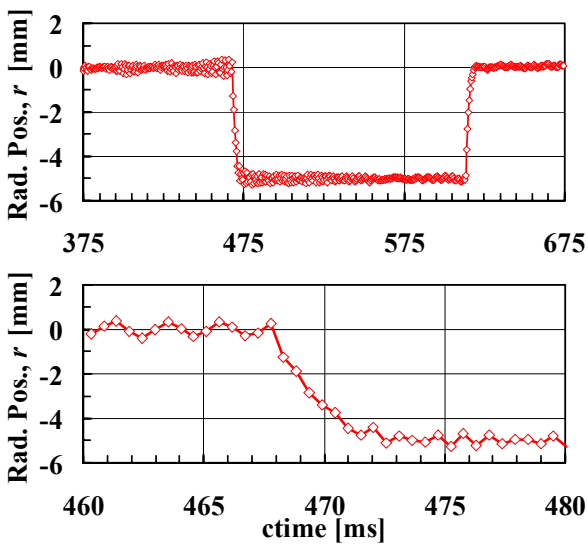

Figure 3: Plots of the DSP-measured radial position as a function of ctime, when a radial steering is applied.

CONCLUSION AND OUTLOOK

A new beam control system for LEIR is being developed. A set of beam tests has been carried out in the PSB and this paper detailed the system setup deployed, both hardware and software, as well as some test results. The tests were successful in their beam control part and validated several new concepts, such as soft-GFAS, DSP-Oasis and soft-timings. The system proved to be very flexible and performant.

From Prototype to LEIR

A new version of the MDDS daughter board will implement a tagged clock scheme, to phase-synchronise all daughter boards' numerically controlled oscillators to a common revolution phase reference. A fanout unit will deliver the tagged master clock over cable or optical fibre.

The beam control system will operate the gap relays of the LEIR cavities [9], to short-circuit them when not in use, thus avoiding beam self-bunching due to cavity impedance.

Capabilities such as a cavity voltage envelope control and a beam ejection synchronisation loop will be added. Three DSP carrier boards, communicating with each other by DSP linkports, will interface with all the hardware. A dedicated real time task will run on the PPC, for remote control and data exchange with the user. Suitable application programs will be developed.

Roadmap After LEIR

After commissioning LEIR, a plan will be finalised to migrate the PSB, Proton Synchrotron and Antiproton Decelerator beam control systems to the LEIR digital scheme, to improve uniformity and maintainability.

REFERENCES

[1] M. Chanel, "LEIR: The Low Energy Ion Ring at CERN", EPAC'02, Paris, June 2002, p. 563.

[2] S. Maury et al, "Ions for LHC: Beam Physics … Challenges", Paper RPPE005, this conference.

[3] M. E. Angoletta et al., "PS Booster Beam Tests of the New Digital Control System for LEIR", CERN/AB-Note-2005-017-RF.

[4] M. E. Angoletta et al., "Feasibility Tests of a New All-Digital Beam Control Scheme for LEIR", CERN/AB-Note-2004-004-RF.

[5] A. Krusche, M. Paoluzzi, "The New Low Frequency Accelerating Systems For The CERN PS Booster", EPAC'98, Stockholm, June 1998, p. 1782.

[6] J. DeLong et al., "Topology for a DSP-Based Beam Control System in the AGS Booster", PAC'03, Portland, May 2003, p. 3338.

[7] G. C. Schneider, "The Phase Pick-Ups and their Signal Transmission in the PSB Beam Control Systems", CERN PS/RF/Note 96-15.

[8] A. Findlay, "PSB Phase Pickup … Modifications for 2001", CERN PS/RF/Note 2001-007.

[9] M. Paoluzzi, "The LEIR RF System", Paper WPAT018, this conference.