DESIGN OF THE APS RF BPM DATA ACQUISITION UPGRADE *

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Abstract

The Advanced Photon Source (APS) is a third-generation synchrotron light source in its tenth year of operation. The storage ring employs three different types of beam position monitor (BPM) systems to measure and control beam motion. The monopulse radio frequency (rf) BPM is a broadband (10-MHz) system, which is considered to be the backbone of orbit control. The rf BPM system was designed to measure single-turn and multi-turn beam positions.

The rf BPMs are presently suffering from an aging data acquisition system. By replacing only the data acquisition we will revitalize this system for another decade and demonstrate a cost-effective approach to improved beam stability, reliability, and enhanced postmortem capabilities. In this paper we present the design of an eight-channel ADC/digitizer VXI board with a sampling rate of 88 MHz (per channel) and 14-bit resolution coupled with a field-programmable gate array and embedded signal processing. We will discuss the upgrade system specifications, design, and prototype test results.

INTRODUCTION

The upgrade uses a three-phase program to replace the data acquisition system since the system is critical to operations. During the first phase, two channels of the data acquisition system were prototyped using the Altera Stratix II™ development kits [1] and Analog Device's ADC [2] evaluation boards. These components were assembled in a 19-inch 2-unit-height rack-mountable cabinet. The data described in this paper was measured from these units. The second phase of this project involves building the first article VXI boards. The plan is to implement one sector or seven BPMs. Phase three will involve instrumenting 280 BPMs that are presently being used in operations.

RFBPM UPGRADE DESIGN

The APS storage ring rf BPM upgrade [3] completely streamlines the data flow though the data acquisition system. The raw data from the receiver is sent directly into the new Fast Digitizing Processor (FDP) VXI card.

The upgrade repartitions the existing system hardware such that the rf section from the button electrodes to the receiver output remains electrically the same and the data acquisition system is replaced as illustrated in the shaded areas in Fig. 1. This approach removes the monopulse receiver from the VXI-based Signal Conditioning and Digitizing Unit (SCDU) [4] and locates it in a designated EMI-shielded chassis. The receiver's center frequency remains at 352 MHz with an intermediate frequency bandwidth of 10 MHz.

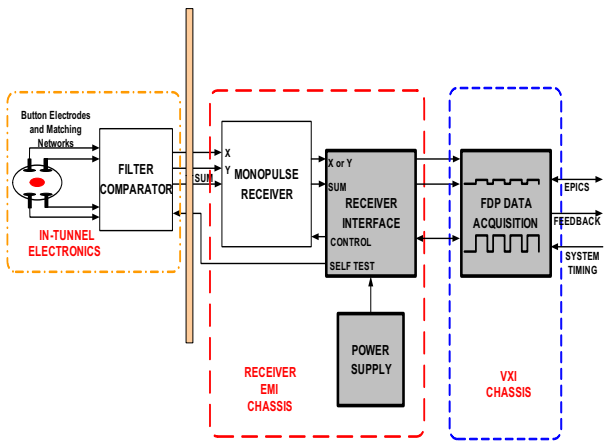

Figure 1: System block diagram.

Receiver Interface

The receiver interface shown in Fig. 1 provides the power supply conditioning and regulation, digital buffers for the receiver control signals (x/y, 0/180), differential drivers for the video signals, and a self-test function. The self-test circuit is a voltage-controlled oscillator with variable gain and a gating feature. The new self test features simulate the various fill patterns used at the APS.

The interface board is mounted to one side of an aluminum chassis and the receiver is mounted to the opposite side. This chassis has an integral heat sink and also provides guides to mount it into a 4-unit-height chassis.

Data Acquisition Front-End Design

The Fast Digitizing Processor data acquisition block diagram shown in Fig. 2 is an eight-channel ADC/digitizer VXI board. A single VXI FDP board will provide the data acquisition for up to four BPMs. The gated integrator and peak detectors used in the old SCDU data processing are replaced by ADCs running at a beam-synchronized frequency of 88 MHz (one quarter of the rf frequency).

The monopulse receiver response was simulated in MatLab [5] to study the effect of receiver output-filter bandwidth on bunch pattern sensitivity. Two different bunch patterns were used for the simulation. The first pattern is designated as 24 singlets and consists of 24

*Work supported by U.S. Department of Energy, Office of Basic Energy Sciences, under Contract No. W-31-109-ENG-38
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single bunches with a maximum current of 4.25 mA each, spaced 153 nanoseconds apart. The second pattern is designated as hybrid 1 and consists of a single bunch containing 5 mA isolated from the remaining bunches by 1.59 microsecond gaps. The remaining current is distributed in eight groups of seven consecutive bunches with a maximum current of 12 mA per group and a spacing of 48 nanoseconds between groups. The simulation was run for both bunch patterns for output bandwidths of 40, 20, and 10 MHz. Averages were computed for a complete turn (324 samples at 88 MHz). The pattern dependence varied from approximately 5% at 10 MHz to approximately 0.1% at 40 MHz bandwidth. In addition, the simulations were run with a notch filter centered at 88 MHz on the output. This filter had no measurable effect on bunch pattern dependence. From the simulations, one can conclude that wider bandwidth reduces bunch pattern dependence, and the addition of a notch filter at the ADC sampling rate provides no additional benefit.

The filter selected for the prototype accepts the differential position and intensity signals from the receiver interface and passes them through three-pole lowpass filters prior to the Analog Devices AD6645 14-bit ADCs shown in Figure 2. The 3-dB cutoff is 40 MHz for the evaluation board. The ADCs have a common clock signal at 88 MHz synchronous to the beam derived by the 44-MHz facility timing.

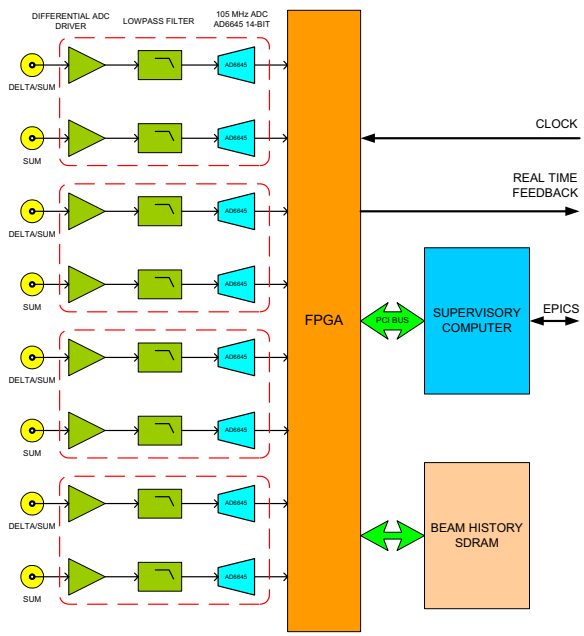

Figure 2: Data acquisition block diagram.

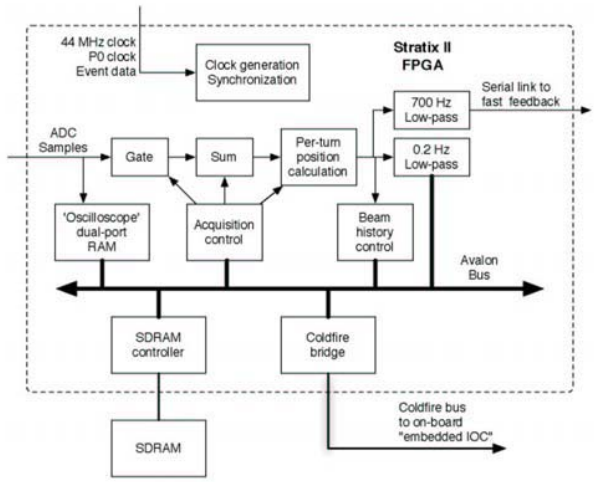

Figure 3: Single channel processing block diagram.

Field Programmable Gate Array

Figure 3 illustrates a single channel for the Altera Stratix II™ field-programmable gate array (FPGA). The clock generation and synchronization block accepts the 44-MHz clock and 'P0' marker from the facility timing system and uses these signals to synthesize an 88-MHz sampling clock to drive the ADCs and a 'beginning of turn' marker to control the calculation of the turn-by-turn position information. This block also contains information about the fill pattern within the storage ring. This information is used to enable the summation block only when valid position signals are present. By performing the gated integration after digitization, the problems of drift and offset in the analog portion of the circuit are avoided. The clock generation and synchronization block drives the commutation and plane select switches within the monopulse receiver front ends to enable data acquisition from either X or Y planes.

The ungated digitized signals are stored in on-chip memory, which can be read by the IOC to provide a 'digital oscilloscope' snapshot of 4096 values of each analog input.

The 'per-turn position calculation' block computes the average value of the gated sum and difference signals for each receiver and for each combination of plane and commutation switch settings.

The turn-by-turn beam position history is stored in a separate SDRAM module. A 128-Mbyte module will allow several seconds of turn-by-turn position information to be recorded.

Communication between the FPGA blocks and the embedded IOC is performed using Altera Avalon™ switching technology. The use of the Avalon "System on a programmable chip" architecture considerably simplifies the task of interconnecting the components within the FPGA. The Avalon system provides a multi-point switching network within the FPGA so that, for example, the beam history FPGA block can be writing information to the SDRAM at the same time as the IOC is reading from the oscilloscope memory.

Feedback

The APS storage ring real-time feedback system [6] needs position data from the FDPs. Presently the real-time feedback system runs at a sample rate of 1534 Hz. Discussions are underway on possible upgrades to that system. The highest sample rate will not exceed 20 kHz and is likely to be near 10 kHz. Position data from the FDPs will not be synchronized with the real-time feedback sample rate. The update rate should be 10 to 20 times the real-time system's Nyquist frequency. For a 20-kHz real-time feedback system sample rate, the minimum update rate from FDPs should be 100 kHz or greater.

Each FDP will provide position data over a fiber optic TAXI [7] link to a module located in the associated feedback crate. This module will provide eight fiber optic inputs to service as many as two FDPs. Initially only four inputs will be used per double sector. The position data will be deposited in registers with one register for each BPM position. The real-time feedback DSPs will then read and process the position data at the feedback sample rate.

SPECIFICATIONS

The original specifications for the rf BPMs quoted in Table 1 are from the early commissioning days and are typically exceeded in routine operation at this time. The monopulse receiver and the evaluation components were tested with 100 mA of stored beam with an equally spaced 24-bunch fill in a top-up mode. The input signals were normalized with four-way combiners in order to correctly represent the beam signal without beam motion. The stored beam resolution of 500 nm in a 0.16-Hz bandwidth was measured limited by receiver intensity dependence between top-up cycles. With this improved data acquisition resolution we can now measure many of the other systematic errors that are related to EMI and temperature drift. The effort spent trying to minimize system resolution has identified many shortcomings. Some of the problems to be addressed will be cable shielding, input line power filtering, cabinet shielding, and temperature regulation. Further testing will continue after the May shutdown to fully quantify the FDP prototype performance.

Table 1: General System Specifications

Parameter	**Specification**	**Prototype**
Single-Shot Resolution	< 200 μm rms	< 10 μm rms
Stored Beam Resolution	< 25 μm rms	< 500 nm rms 0.16 Hz BW ≥ 24 bunches
Real Time Feedback, Resolution	New 100 Hz BW <TBD degree shift >100 KHz update	Not measured
Dynamic Range, Position	±20mm Minimum	±10mm Minimum
Dynamic Range, Intensity 0.1-10 mA	< 200 μm deviation	Not measured
24 Hour Stability	± 30 μm rms	± 10 μm rms

ACKNOWLEDGMENTS

The authors would like to acknowledge John Carwardine, Glenn Decker, and Om Singh for many helpful discussions.

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