DIGITAL BEAM POSITION MONITOR FOR THE HAPPEX EXPERIMENT*

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Abstract

The proposed HAPPEX experiment at CEBAF employs a three cavity monitor system for high precision (1um), high bandwidth (100 kHz) position measurements. This is performed using a cavity triplet consisting of two TM110-mode cavities (one each for X and Y planes) combined with a conventional TM010-mode cavity for a phase and magnitude reference. Traditional systems have used the TM010 cavity output to directly down convert the BPM cavity signals to base band. The multi-channel HAPPEX digital receiver simultaneously I/Q samples each cavity and extracts position using a CORDIC algorithm. The hardware design consists of a RF receiver daughter board and a digital processor motherboard that resides in a VXI crate. The daughter board down converts 1.497 GHz signals from the TM010 cavity and X and Y signals from the TM110 cavities to 3 MHz and extracts the quadrature digital signals. The motherboard processes this data and computes beam intensity and X-Y positions with resolution of 1um, 100 kHz output bandwidth, and overall latency of 1us. The results are available in both the analog and digital format.

INTRODUCTION

Two upcoming parity-violation experiments (HAPPEX) require strict beam parameters and precise instrumentation in order to minimize systematic errors to acceptable levels [1]. One such constraint is the position measurement of the beam, to 1um, while it is undergoing a 30 Hz spin flip as well as being rastered at 25kHz. The beam centroid is calculated during each 33 ms period. Conventional switched-electrode electronic stripline beam position monitors (SEE BPMs) at CEBAF lack the resolution and output bandwidth for such a measurement [2]. A cavity-based triplet system has recently been used for other experiments which employs a pair of orthogonal TM 110-mode cavities to obtain displacement, and a standard TM 010-mode beam current monitor (BCM) cavity to establish amplitude and phase reference. The basic advantage is voltage amplification achieved from a high-Q resonant structure [3]. Typical beam conditions for the HAPPEX experiment include 10-100 uA, with potential displacements of up to 5 mm, resulting in a dynamic range of 60 dB as predicted by MAFIA models. Precision measurements can be accomplished with an analog front end down converter followed by an FPGA-based digital processor implementing quadrature IF sampling and processing techniques. Quadrature components are first filtered, and subsequently X and Y phase and amplitude are extracted. Position magnitude is normalized to the current cavity phase and magnitude, and assigned a quadrant, resulting in a signed output. Phase offset and adjustable gain are provided by an EPICS interface to normalize X and Y, which is useful for finding cavity center and performing calibrations. Additional interfacing permits a host computer to set calibration parameters over the VME/VXI bus.

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THEORY

Cavity BPM systems have been used by other laboratories, whereby the BCM output is used as a Local Oscillator (LO) in order to homodyne the X and Y cavity outputs to baseband, obtaining displacement information. This scheme is quickly becoming antiquated due to relatively expensive (and often obsolete) RF components, large systematic effects (i.e. offset and gain), 1/f noise associated with DC detection, as well as inability to re-configure in the field.

The HAPPEX receiver utilizes a 3 MHz intermediate frequency (IF) which is easily oversampled by an ADC, as shown in Figure 1, and the associated phase and amplitude information is extracted numerically. In addition, the receiver architecture is relatively generic, supporting on-the-fly configuration as necessary, consistent with the emerging software-defined radio (SDR) philosophy.

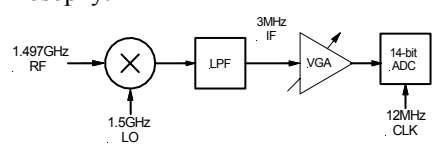

Figure 1: RF Front end downconverter.

The 3MHz IF signal is amplified by a variable gain amplifier (VGA), sampled at a 12MHz rate and demodulated into quadrature components (I, Q). By oversampling, as shown in Figure 2, the input is sampled at 90^{o} intervals, such that the data stream is a repeating pattern of I, Q, -I, -Q with an effective sample rate of 6MSPS. Alternate samples represent the real (I) and imaginary (Q) components of the RF input signal [4]. The VGA is digitally controllable via the FPGA/VME, and is used to provide good dynamic range, and also limit the maximum signal to prevent over ranging by the ADC.

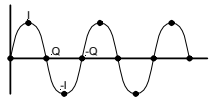

Figure 2: 4X I/Q sampling.

Once the I/Q demodulation is performed, a Gaussian filter is employed as a halfband filter to gracefully limit the input bandwidth to ~500 kHz, permitting decimation. The cavity, itself, provides ~1MHz of analog anti-aliasing filtering. A Gaussian response has good immunity to ringing and overshoot, desirable qualities for a high dynamic range signal produced by a rastered beam. The filtered output is decimated by 6 to produce a 1 MSPS output data rate. A Kaiser Window filter was chosen for the 75 kHz narrowband filter because of its superior transient performance. Combined with the Gaussian filter, no measurable overshoot was observed with the SystemView & Matlab model, as well as bench tests. Output sample rate is then decimated to 250ksps to comply with 75 kHz output bandwidth Nyquist criteria with headroom.

Phase and amplitude detection are accomplished by using a CORDIC routine for each of the three channels, whereby the video vector is iteratively rotated to align with the real (I) axis [5]. The resultant I magnitude value is representative of the signal intensity, hence displacement, while the number of iterations is proportional to the phase of the signal. The routine is a fast and clever way of calculating $x^2 + y^2$ and tan-1(y/x).

IMPLEMENTATION

The daughterboard contains a three-channel 1.497 GHz receiver and a 1.500 GHz synthesizer. The RF input at 1.497GHz is down converted by the synthesizer to produce a 3MHz IF. The 1.5GHz is frequency and phase locked to the Master Oscillator (MO) reference 10 MHz signal, resulting in synchronicity between all cavity channels and the accelerator. In addition, the 12 MHz sample clock (which resides on the motherboard) for the ADC is also MO-derived.

The VXI motherboard contains the digital electronics necessary to process digital signals to and from the daughterboard, interface to the VXI bus, and 10/100 Ethernet [6]. As shown in Figure 3, the board features one Altera Stratix FPGA, 64Kx16 DPRAM, 1Mx32 RAM, 1Mx32 FLASH, Phase Lock Loop (PLL), six 16-bits 500K-sample DACs, 10/100 Ethernet, general purpose digital IO, and infrared input and output. The motherboard uses two 100-pin and two 20-pin stackable connectors to support daughter board(s). Each 100 pin connector has 70 digital I/O, PLL clock output, FPGA clock input, and digital powers. Each 20 pin connector provides VXI analog powers (+/-12V, +/-24V).

We chose an Altera Stratix FPGA with 18,000 to 25,000 logic elements (LE are the basic electronics building blocks), 80 eight-bit multiplier/ accumulators, and can support both hard coding and a soft microprocessor core (NIOS) simultaneously.

Care was taken in the design of the clock PLL to achieve a jitter of less than one picosecond. The PLL takes in an analog (or digital) signal from a front panel SMA connector and generates a square wave that is phase locked to the input. The clock signal is double buffered

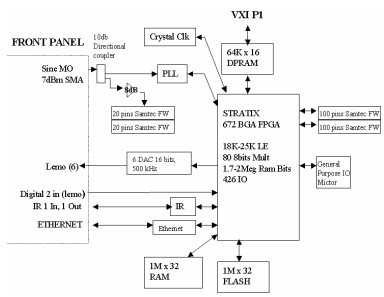

Figure 3: Motherboard components.

and distributed to the FPGA and to both 100-pin connectors. The signal from the SMA connector is buffered and distributed to both 20-pin connectors.

Firmware for the receiver, as shown in Figure 4, rotates X and Y channels by an amount equal to the BCM phase, plus an arbitrary offset, such that a quadrant determination can be performed. The algorithm is sensitive to the 180-degree phase inversion of the X and Y signals as the beam traverses the cavity boresight [7]. The value of the offset must be found empirically; using beam scans, and represents the "electrical center" of the BPM cavities.

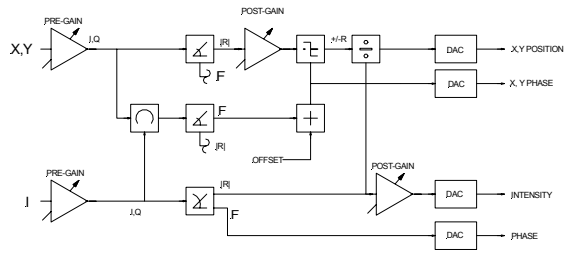

Figure 4: Firmware functional block diagram.

X and Y are then normalized by dividing the resultant with the intensity magnitude. Finally, signed positions are produced and sent to a 16-bit, 1 MSPS DAC, as well as output to EPICS, which also controls the entire receiver operating parameters.

Operationally, individual channel gains are used to set an output DAC full-scale reading for a given displacement and beam current. For S/N > 10dB, phase determination is quite solid. However, as S/N approaches ~3dB, spontaneous 180^o phase flips will occur, known as "click noise," becoming significantly worse for degrading signal conditions [8].

RESULTS

Bench tests were performed prior to installation in the CEBAF accelerator using input levels suggested by MAFIA cavity modeling. This gave good indications of algorithm behavior, as well as an opportunity to become familiar with operational aspects of the receiver and EPICS interface. In-situ measurements were made, both parasitically, and with formal test plans. The test plans included moving the beam in the Y-direction by known amounts (verified by other calibrated beam line components), in an effort to extract resolution, dynamic range, and linearity. The results are shown in Figure 5. In

addition, comparisons of measured beam current were also performed, such that insensitivities to beam intensity could be demonstrated (Figure 6), as well as overall ability to measure absolute current with 1% absolute accuracy, when compared with a high-precision BCM already installed (Figure 7). Finally, Figure 8 is a measure of crosstalk between X and Y (only Y position was moved), demonstrating good orthogonality and low channel-to-channel crosstalk.

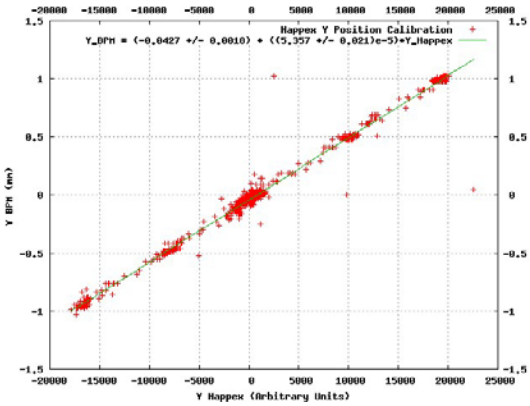

Figure 5: Calibration of the HAPPEX Y measurement against an existing BPM.

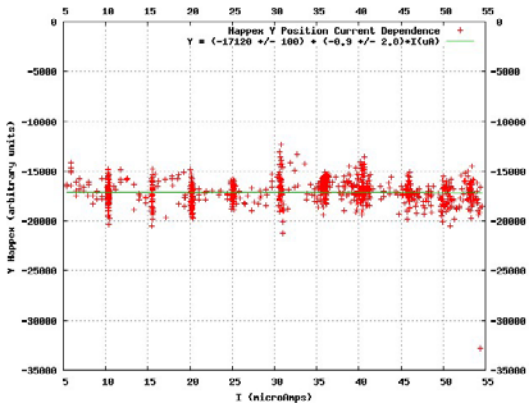

Figure 6: The Y position stayed constant as the current was changed from 1uA to 55uA.

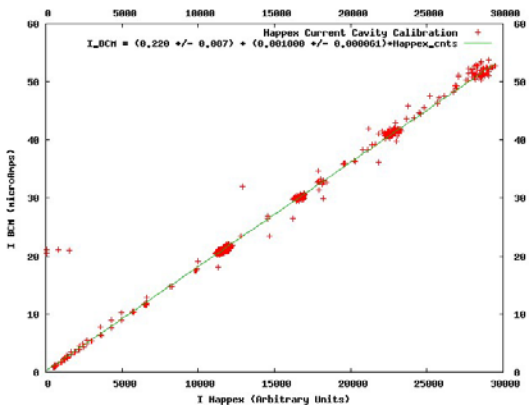

Figure 7: Calibration of the I cavity against the existing BCM cavity.

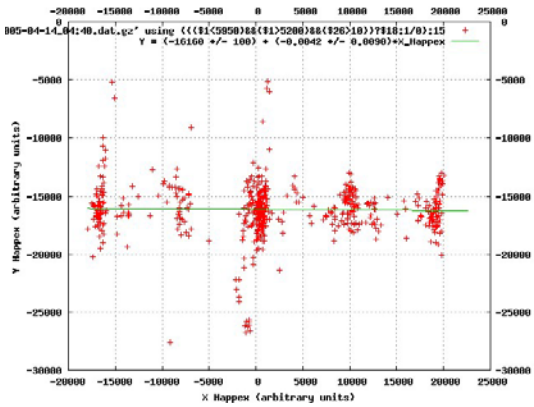

Figure 8: The X position was varied by ± 2mm and no change observed on the Y position.

SUMMARY

The results of the beam-based test plans, combined with the parasitic data collection were completely consistent with the bench tests, and verified compliance with the requirements. In addition, the SDR architecture provided a platform on which to test other filter schemes and algorithms for parallel projects. A user-friendly EPICS control interface permits operators to use the system without a rigorous understanding of the firmware. Finally, the quadrature sampling technique has since been applied using slower clock rates, thereby intentionally aliasing but preserving the amplitude and phase information.

REFERENCES

[1] D. Armstrong, D. Lhullier, R. Micheals, K. Paschke, "Specifications of Beam Parameters for HAPPEX-II and HAPPEX-He," HAPPEX Collaboration Technical Paper, Sept. 11, 2003

[2] T. Powers et. al.: "Design, Commissioning, and Operational Results of Wide Dynamic Range BPM Switched Electrode Electronics," Proceedings of the 7th Beam Instrumentation Workshop, Argonne, IL

[3] R. Lorenz, S. Sabah, H.J. Schreiber, H. Waldman, "Cavity-type Beam Position Monitors for the SASE FEL at the TESLA Facility," TESLA-FEL2003-03, 2003, May 28, 2003

[4] C. Ziomek and P. Corredoura, "Digital I/Q Demodulator" Proceeding of the 1995 Particle Accelerator Conference

[5] R. Andraka, "A Survey of CORDIC Algorithms for FPGA Based Computers – Proc of the 1998 CM/SIGDA Sixth International Symposium on FPGA's, February 22-28, 1998, Monterey, CA

[6] C. Hovater et al, "A New RF system for the CEBAF Normal Conducting Cavities" LINAC 2004 Conference Proceedings, Lubeck, Germany August 2004

[7] R. Ursic, R. Flood, C. Piller, E. Strong, L. Turlington, "1nA Beam Position Monitoring System," Proceedings of the 1997 Particle Accelerator Conference

[8] Digital and Analog Communication Systems, 3rd Edition, L. Couch, 1990 Macmillan Publishing Company, NY, NY

