# A BUNCH-BY-BUNCH AND TURN-BY-TURN INSTRUMENTATION HARDWARE UPGRADE FOR CESR-c*

M. A. Palmer†, J. A. Dobbins, C. R. Strohman and E. P. Tanke, LEPP, Cornell University, Ithaca, NY 14850, USA

*Abstract*

A key factor in the colliding beam performance of the Cornell Electron Storage Ring (CESR) is the impact of parasitic beam-beam interactions between bunches in the two beams as they follow their electrostatically separated orbits in a single vacuum chamber. In order to better investigate the differential performance of bunches in CESR, instrumentation electronics has been developed to allow acquisition of turn-by-turn data from multiple bunches simultaneously. The electronics consists of a standardized digital board centered around an Analog Devices TigerSHARC family digital signal processor, a communications interface, and an interface to the CESR Precision Timing System. Mated to these components is an analog front-end and digitizer board which is customized for the particular diagnostic device of interest. Front-ends have been developed for beam position monitor, luminosity monitor, and beam profile monitor applications. We describe the design and characterization of this new hardware.

## INTRODUCTION

CESR presently operates in 2 energy regimes, at beam energies of 1.5–2.5GeV for CLEO-c high energy physics and at a beam energy of 5.3GeV for synchrotron light source operations. In both cases, counter-rotating beams of electrons and positrons share the same beam pipe. The closed orbits of the two species are electrostatically separated so that there is only a single interaction point, inside the CLEO detector, where the bunches collide. Several effects can contribute to variations in environment between bunches. For instance, the accumulated long range beam-beam interactions experienced by the bunches at the parasitic crossing points around the ring varies according to bunch. In order to maximize time-integrated performance, whether it be for luminosity or for X-ray intensities, CESR typically operates in a regime where significant variations in performance between bunches [1] are present. Understanding these bunch-to-bunch variations is critical for optimizing CESR performance through the remainder of its scheduled high energy physics operation.

We have previously described the implementation of single-bunch, turn-by-turn readout for a set of beam position monitors (BPMs) in the CESR ring [2]. Our present efforts focus on the extension of this capability to parallel multi-bunch readout of BPMs as well as other fast instrumentation devices coming into use at CESR. These other devices include a fast radiative-Bhabha luminosity monitor [3] (FLM) and beam profile monitor (BSM). Our basic design criteria for reading out these devices are as follows:

- 72MHz digitization to capture 14ns spaced bunches
- On-board data-buffering sufficient to accommodate 10000 turns of data from 45 parallel-sampled bunches
- On-board data processing capability to provide automatic timing control, gain control (BPM applications), and pre-processing of the raw data before transfer to the CESR Control System
- Modular front-end support to accommodate different detector technologies

These devices offer a new window on bunch-to-bunch dynamics and performance at CESR. In the following, we describe the architecture and results obtained from initial prototyping tests with the new multi-bunch electronics.

## DESIGN ARCHITECTURE

Fig. 1 provides an overview of the data acquisition hardware architecture. The hardware consists of a digital motherboard with connectors for four analog boards, a timing board, and an I/O transition board. An external clock receiver module connects to the CESR timing system. The digital board has an Analog Devices TigerSHARC TS101 digital signal processor (DSP), a Xilinx Virtex-2 field programmable gate array (FPGA), 2 Mbytes of static RAM, and 512 kbytes of FLASH memory. The FPGA contains the logic for external communication, extraction of data encoded on the CESR timing signal [4], address decoding and bus sharing, and data acquisition control.

The timing board receives the CESR 24MHz clock signal that has an encoded turn marker with shaker phase information for betatron phase measurements, trigger signals, and a command word. A phase-locked loop (PLL) extracts the 24MHz clock. A second PLL multiplies the clock signal by three to produce a 72MHz clock. Two identical delay blocks are provided. Each has two tapped delay lines that can delay the 72MHz clock in 10ps steps. The delayed clock is sent to four additional delay lines with 10ps steps that provide a clock signal to the ADCs on each analog card. These four delay lines can compensate for variations in cable length or electronic delays, so that the ADC conversions can be done at the peak of the analog pulse.

Two types of analog boards have been developed. The first, for BPM applications, has a single input and filter that drives two identical digitization blocks. One block is used for electrons and the other for positrons. Each block

* Work supported by the National Science Foundation
† map36@cornell.edu

 

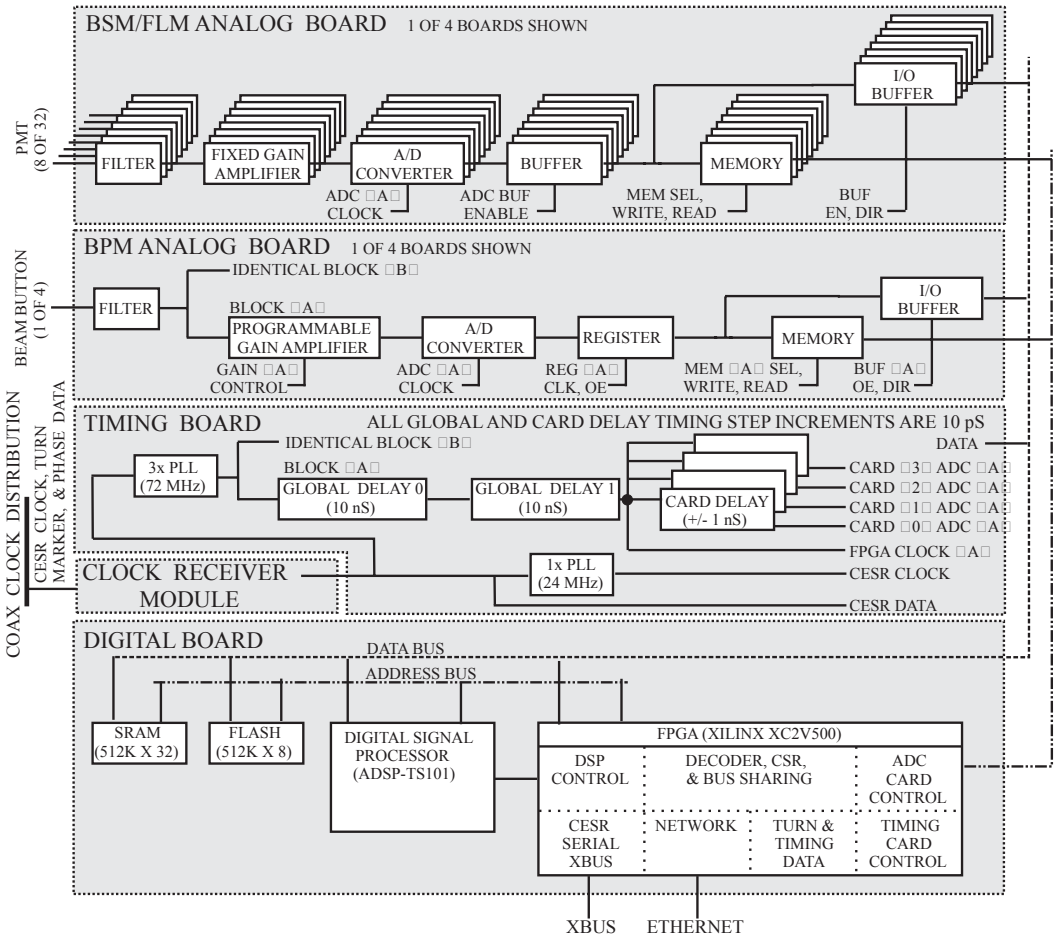


Figure 1: Architecture Overview

has a programmable gain amplifier (AD8369), analog-to-digital converter (AD9245), temporary data register, and 512 kwords of memory. The digitization times of the two analog-to-digital converters (ADCs) are set independently on the timing board. However, there is only a single address bus for the memory, so judicious settings of the register clocks and memory write strobe timing are required to meet the data setup and hold times at the memory.

The second type of analog board, for photomultiplier (PMT) applications, has 8 inputs. Each input connects to a fixed gain amplifier (OPA842 for FLM; OPA847 for BSM), differential ADC driver (AD8131), ADC (AD9235), and 512 kwords of memory. The amplifier gains are set with resistors. All 8 ADCs convert at the same time. The memory address bus to the analog boards is separate from the general purpose address bus on the digital board. This allows normal bus activity while data is being collected, with the constraint that data cannot be read from the analog boards while acquisition is in progress.

## PROTOTYPE TESTING

Fig. 2 shows the basic front-end for PMT readout. 2 configurations have been implemented and tested: the first for readout of Hamamatsu R7400U PMTs used in the FLM; and the second for readout of a Hamamatsu H7260K linear PMT array (32 channels with 1mm pitch) being tested for the BSM. Fig. 3 shows FLM luminosity counting rates ob-

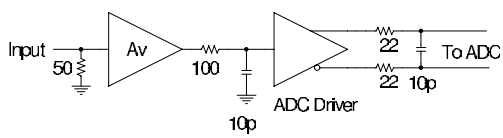


Figure 2: FLM/BSM front-end layout.

tained for five bunches in a single train during the most recent CLEO-c run. Note the range of performance between bunches for fully tuned operations. Fig. 4 shows prototype data obtained with the BSM device. Synchrotron light was brought to the PMT by picking off a portion of the light beam from our existing $e^-$ beam profile monitor with a beam-splitter, then inserting a $500\pm25\mathrm{nm}$ filter and a cylindrical defocusing lens so that the size of the band of light on the PMT face should be $\sim 3.6\times$ larger than the source. Part (a) of Fig. 4 shows signals obtained at 14 ns intervals during a period of $8\times5$ running. All 40 bunches are clearly visible. Plot (b) shows a profile measurement obtained for a single bunch. The statistics in the single bunch profile correspond to integration of 500 turns.

Fig. 5 shows the dual amplifier front-end configuration

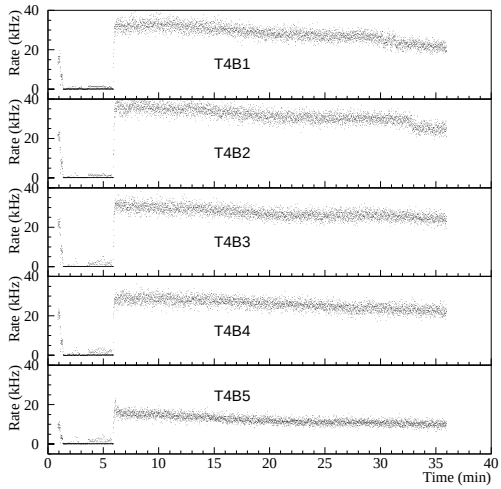


Figure 3: FLM bunch luminosity data for all bunches in a single train (Train 4).

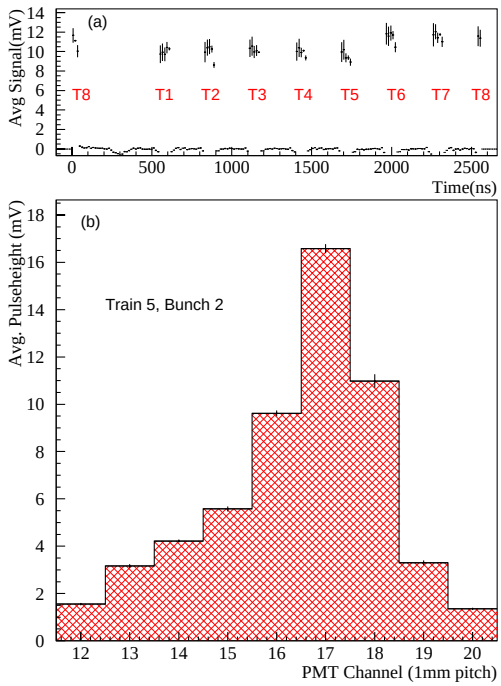


Figure 4: BSM prototyping data: (a) Timing scan showing the CESR $e^-$ bunch structure during synchrotron light source operations (9400 turns per point); (b) Beam profile data obtained for a single $e^-$ bunch for 500 turns as observed on the central PMT channels. The vertical scale for each plot is in units of the voltage produced at the PMT output termination.

being tested for simultaneous $e^+$ and $e^-$ BPM readout. The initial front-end filter configuration is the same as that employed in our existing turn-by-turn system, however, the present digital variable gain amplifier and digitizer are higher bandwidth versions. We intend to explore the operational limits of increasing the filter bandwidth, for better sampling at ring locations where passage of the electrons and positrons is closely spaced in time, in the immediate future. Timing scan data of a beam signal is shown in Fig. 6. It is in good agreement with the PSpice simulation shown in the same figure.

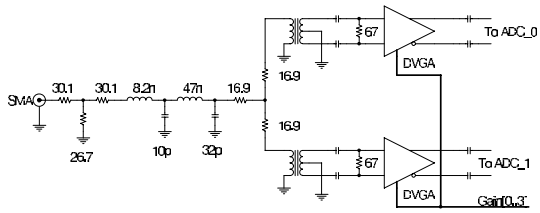


Figure 5: BPM front-end layout.

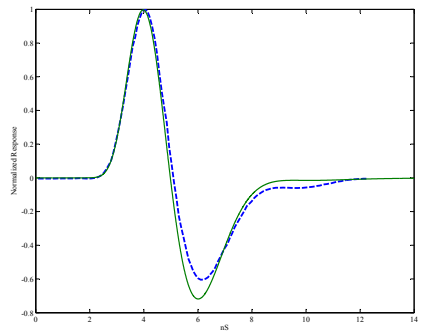

Figure 6: BPM front-end signal response. A PSpice simulation is shown by the solid (green) line while the prototype front-end data is shown by the dashed (blue) line.

## CONCLUSIONS

Initial prototype data obtained with our new multi-bunch electronics appears promising. Efforts are presently underway to obtain further operational data with these devices, to develop on-board data-processing algorithms, and to fully integrate them into the CESR control system.

## ACKNOWLEDGMENTS

We would like to express our thanks to the LEPP Electronics Shop for help in assembly and installation of the prototype devices and D. Hartill for his help with the beam profile monitor.

## REFERENCES

[1] D. Sagan *et al.*, "Effect on Luminosity from Bunch-to-Bunch Orbit Displacements at CESR", Proc. of the 2001 IEEE Part. Accel. Conf., p.347.

[2] M. Palmer *et al.*, "An Upgrade for the Beam Position Monitoring System at the Cornell Electron Storage Ring", Proc. of the 2001 IEEE Part. Accel. Conf., p.1360.

[3] M.A. Palmer *et al.*, RPAT062, these proceedings.

[4] M. Palmer *et al.*, 'System Level Implementation of Beam Position Monitors with Local Data Processing Capability for the Cornell Electron Storage Ring'", Proc. of the 2003 IEEE Part. Accel. Conf., p.2473.