PROTOTYPE DIGITAL BEAM POSITION AND PHASE MONITOR FOR THE 100MEV PROTON LINAC OF PEFP*

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Abstract

The PEFP (Proton Engineering Frontier Project) at the KAERI (Korea Atomic Energy Research Institute) is building a high-power proton linear accelerator aiming to generate 100-MeV proton beams with 20-mA peak current (pulse width and max. repetition rate of 1 ms and 120 Hz respectively). We are developing a prototype digital BPPM (Beam Position and Phase Monitor) for the PEFP linac utilizing the digital technology with field programmable gate array (FPGA). The RF input signals are down converted to 10 MHz and sampled at 40 MHz with 14-bit ADC to produce I and Q data streams. The system is designed to provide a position and phase resolution of 0.1% and 0.1◦ RMS respectively. The fast digital processing is networked to the EPICS-based control system with an embedded processor (Blackfin).

INTRODUCTION

The PEFP accelerator has been designed to accelerator a 20mA proton/H- with the final energy 1GeV super-conductive linear accelerator. The 20MeV proton accelerator is constructing in the PEFP test facility, and will be commissioned in 2005. After the commissioning, PEFP test facility will provide the proton beam for the many industrial applications. With the technologies developed in PEFP test facility, the 2nd phase accelerator of 100MeV energy will be constructed in 2010. Presently it aims to achieve 100MeV beam energy with 20mA(peak, 1-mSec macro-pulse duration) beam current. Refer to Table 1 for major beam parameters of the PEFP accelerator.

Table 1: Beam Parameters of PEFP/KAERI Accelerator

	Operation Mode	NOTE
	Pulse	
Beam Energy	3 – 20 - 100MeV	BPM Operation Region
β	0.08 – 0.20 – 0.43	
V	1.003 – 1.021 – 1.107	
Average Beam Current(I_{av})	Peak 20mA	
Pulse Width(mS)	few	
Bunch Length	160pS	PARMILA Simulation Result
Bunching Frequency	350MHz	

*Work supported by PEFP, KAERI, KOREA…
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The BPPM(Beam Position & Phase Monitor) electronics has been developed by the Bergoz Instrumentation in accordance to our specification. It is a full-analog processor that is based on the Bergoz Log-Ratio BPM electronics for beam diagnostic of the 100MeV proton linear accelerator. We are going to develop the digital beam position & phase monitor based on recent digital technology available for the better measurements. One of the advantage of the ongoing digital BPPM is to take mainstream solution using a FPGA & a embedded Processor. Another advantage is to make the hardware platform modular to simplify the design and testing as well as to provide a more general purpose instrumentation platform for other diagnostic such as beam current monitors. Required specifications for the BPPM electronics are shown in Table 2.

Table 2: Specification of BPPM electronics for the PEFP/KAERI Accelerators

	POSITION	PHASE
Operating Frequency	350MHz	←
Induced Signal(min.)	-57.5dBm@100MeV	←
Induced Signal(Max.)	-4.56dBm@3MeV	←
Resolution & Stability	< 50μm@20mmØBeam Pipe	< ± 1deg.
Operation Modes	CW or Pulsed	←
Output Signal Bandwidth	> 5MHz	←

It should provide the resolution and stability<50um(at 20-mm Diameter beam pipe) for the position measurement and <+/- 1.0degree in the phase measurement. Since the PEFP linac was designed to operate in both CW and pulsed modes, one of the most important requirements for the BPPM electronics was that it should provide position and phase measurements for the two operation modes of the accelerator.

HARDWARE DESIGN

The digital BPPM operates by down converting the four individual BPM PU button signals which are a 350MHz to an IF of 10MHz. These IF signals are sampled at 40MHz to generate the quadrature information that is processed to measure beam position and phase.

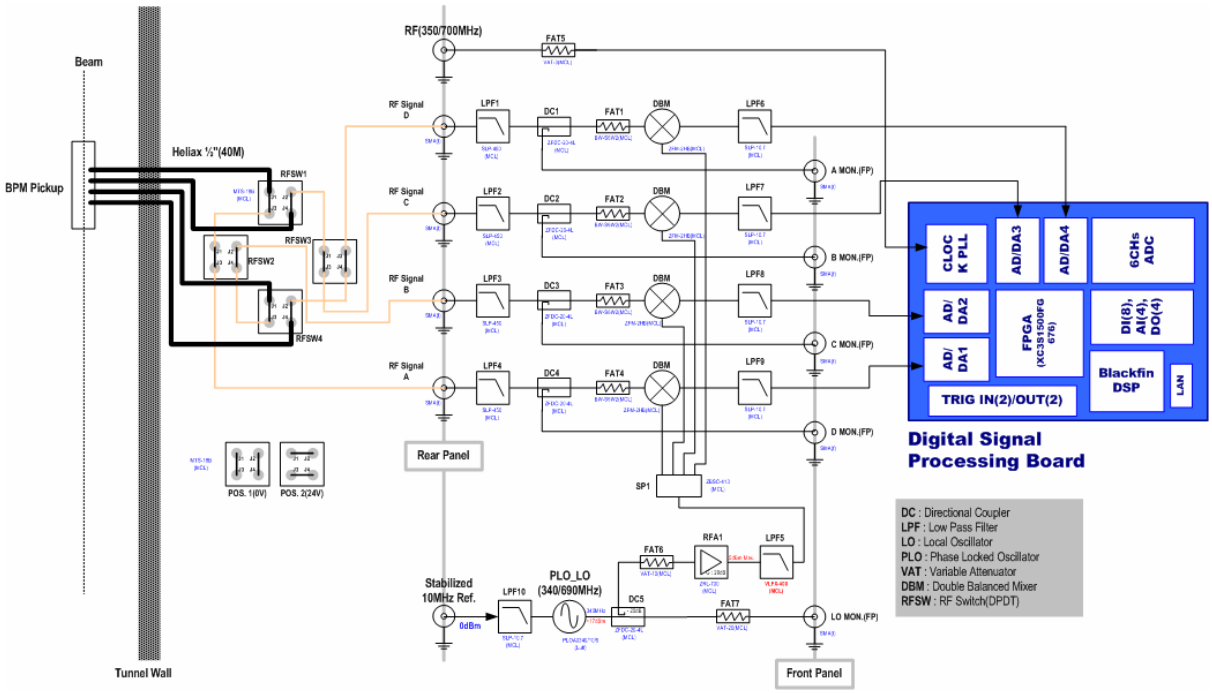

Figure 1: A configuration of the Digital Beam position and Phase Monitoring

The block diagram of the digital BPPM for PEFP Linear accelerator is shown in Figure 1. A synchronized clock signal(80MHz LVPECL) generation is serially-programmed to accommodate the optimised clock signal frequency. The beam position and phase resolution depend on the ADC sampling clock jitter relative to the various RF sources in the system. Figure 2 shows the performance of the PLL clock generator on the digital BPPM core board.

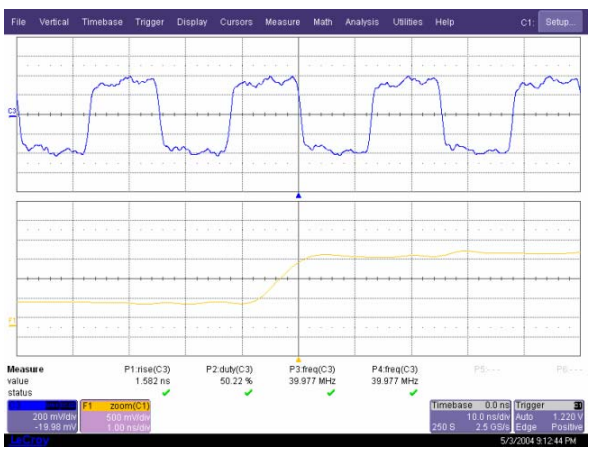

Figure 2: The characteristic of the PLL clock generator

The RF parts contains four channels of down conversion using a local oscillator distribution chain with RF amplifier, PU signal monitor using a directional coupler and the synchronized PLL clock generation by the reference signal from master oscillator. The digital processing board has also 4channels of 14-bit ADCs clocked at 40MSPS.

A single 1U high 19" shielded enclosure contains RF chains and the core board including with a embedded processor(Analog Devices's Blackfin ADSP-BP533-SBBC500) as shown figure2. The four 14-bit

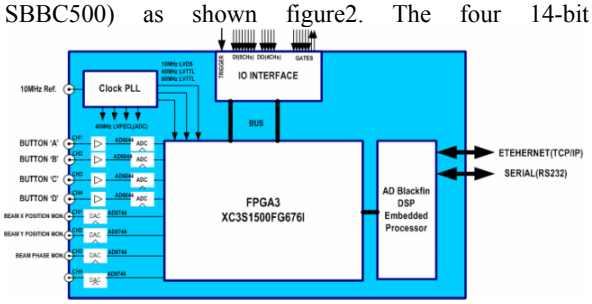

Figure 3: The detailed configuration of the Digital BPPM Core Board

ADCs(AD6644) operated at 40MS/s, and two 14-bit DAC(AD9744) operated at 80MS/s. A FPGA(Xilinx Spartan3 XC3S1500FG676C) provides signal processing path, and connects to an embedded processor. The phase lock loop circuitry, base on an ADF4001, can lock the on-board voltage controlled crystal oscillator(VCXO, 80MHz Connor-Winfield VPLD54TE) to an external source. In our case, that source is a 10MHz stable referenced IF signal from master oscillator.

The embedded processor board provide the direct interface to the control register and hardware. A network host computer connects the fast signal-processing chip to outside world via Ethernet. Timing and interlocks are routed through an FPGA. This feature is purposefully independent of, and not over-ridable by the FPGA and the

embedded processor. The circuit design is based on a design for PEFP LLRF digital RF control system. Figure 3 shows the photograph of the prototype digital BPPM.

Figure 4: The photograph of the prototype digital BPPM

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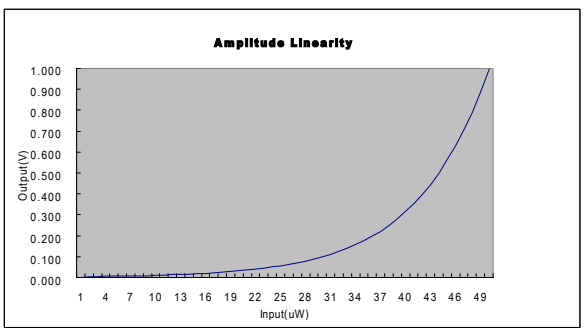

Figure 5: RF signal (350MHz Carrier) amplitude linearity of the prototype digital BPPM

Figure 5 shows the amplitude sampling linearity of the carrier(-50 to -2dBm at 350MHz).

SUMMARY & NEAR FUTURE PLAN

We are developed the prototype digital beam position and phase monitor based on stand-alone hardware and software. In the near future, the local test of the digital BPPM is going to use lookout software at personal computer basis on windows OS. And EPICS control system will be connecting to be confirmed the performance of the digital BPPM on local condition. A windows OS system will be used as an integrated development environment in order to make it easy for us to develop the software of FPGAs, DSPs and a CPU host.

Further improvement of the performance is being studied.

ACKNOWLEDGMENT

We would like to deeply thank S. Yamaguchi, S. Michizono in KEK and Lawrence Doolittle, Alessandro Ratti in LBNL who gave much help and information.

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