TIMING SYSTEM FOR J-PARC

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Abstract

J-PARC has three accelerators running at the different repetition rates; a 400-MeV linac (50Hz), a 3-GeV rapid cycling synchrotron (RCS, 25Hz), and a 50-GeV synchrotron (MR). The linac and the RCS deliver the beam pluses to the different destinations in each cycle. The destinations are scheduled according to the machine operations. We define two kinds of timing, "scheduled timing" and "synchronization timing" so that the accelerators are operated with proper timing and the beam pulses are transported to the experimental facilities or the next accelerators. The J-PARC complex requires a stable and precise timing system. The system is based on a master clock generated by a synthesizer and the triggers are operated independently of the AC-line frequency. We describe the design of the J-PARC timing system and their configuration, and also present the hardware details.

INTRODUCTION

J-PARC [1, 2] is a project of high-intensity proton accelerator complex which produces MW-class high power proton beams. The complex consists of 400 MeV linac, 3-GeV Rapid cycling synchrotron (RCS), and 50-GeV synchrotron (MR). A stable and precise timing system is a key system to accelerate the ultra-high intensity proton beam.

The accelerators have different repetition rates. The linac, RCS and MR are operated at 50 Hz, 25 Hz and 1/3.64 Hz, respectively.

Each pulse of the linac and the RCS has different destination. The linac is operated for the RCS and the accelerator-driven nuclear transmutation (ADS) alternatively. Also, four pulses of the RCS in the 91 pulses in the MR cycle are lead to the MR and the others are delivered to MLF (Material and Life Science Facility). Thus, the linac and the RCS are operated in different modes and timing according to the destinations. The beam destinations of the accelerators are scheduled.

Two kinds of the timing are defined for the J-PARC: "scheduled timing" and "synchronization timing". The scheduled timing is defined by a delay from the 50 Hz *trigger clock* sent from the central timing control. The synchronization timing is based on the trigger generated by the accelerator device other than the central timing control. The 50 Hz trigger is generated independently of the AC-line, by using the master clock generated by the high-stability synthesizer.

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We describe the operation principle and the hardwares of the scheduled timing and the concept of the synchronization timing. Also we discuss on the advantages and the possible impacts of the non-line-synched operations.

SCHEDULED TIMING

Operation Principle

In Figure 1 the operation principle of the scheduled timing is illustrated. In the scheduled timing the trigger is defined as a delay from the 50-Hz trigger clock sent from the central timing control to the facilities. A control word (so-called "type" which presents the operation type of the accelerator during the next 50-Hz period) is broadcasted to the receiver-modules for the target devices in the J-PARC facilities, before the trigger clock is sent from timing-control. Each receiver module has own memory which determines the behavior during the next period according to the type information. The receiver module works in compliance with the received type as follows:

- The receiver outputs a trigger pulse at a programmed delay. In Figure 1 the "Receiver module 1" output pulses at delays of "Delay-1A" and "Delay-1B" for "Type-A" and "Type-B" respectively.
- It suppresses the pulse output during the next period. In the figure, the "Receiver module 4" does not output a trigger pulse when "Type-A" comes.
- Also, it continues the delay-counting beyond the trigger clock. The "Receiver module 3" does not reset the counter with the trigger clock when the "Type-B" is received. If the counter reaches to the programmed value, the receiver outputs a pulse.

The target devices can run at the different timing and modes in each 50-Hz period with the scheme above. One type-sequence corresponds to one MR cycle.

Hardwares for the Scheduled Timing

The following modules are in the central timing control. A high-stability synthesizer and the *master clock generator* generate the master clock. The master clock frequency is to be 12 MHz, since the linac accelerating frequency 324 MHz can be deviled by 12MHz. The *trigger clock generator* outputs the 50 Hz trigger clock by counting the master clock. The *timing control transmitter* module sends type information every 50Hz period according to the accelerator operation. The maximum length of the type-sequence

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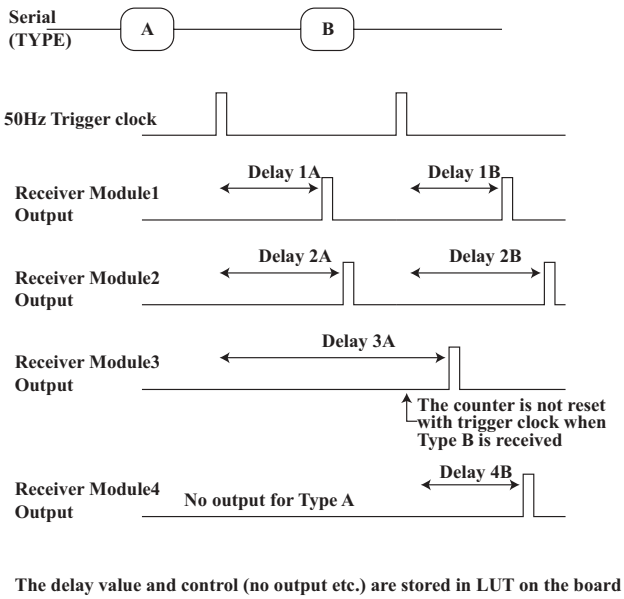

Figure 1: Operation principle of the scheduled timing.

is 1024. The type is serialized. The type-sequence is set from the remote.

A fanout and E/O modules are used for the signal distribution to the J-PARC facilities. This star-configuration distributes the same clocks and the information to all facilities. Optionally, a relay station is configured by using a set of an O/E, a fanout and E/O modules.

The timing receiver panel is illustrated in Figure 2. The O/E module converts the optical signals from the central timing control into the electrical signals. The converted clocks and type are led to the *timing control receiver* module, which generates the delayed pulses.

The receiver module has a look-up table (LUT), which contains *delay words* (delay value and control bits). The delay words are downloaded into LUT from the remote. The receiver picks up the delay word from the LUT according to the received type. By the delay words the behavior of the receiver is defined as the three ways as described in the previous subsection. The internal counter clock is 96 MHz which is generated from the 12 MHz master clock and the counter width is 24-bit; the receiver can count up to about 170 msec. A receiver has eight output channels. The receiver is a VME module and can generate VME interrupts according to the delay words.

The *trigger fanout* and *gate fanout* modules convert the signal level of the pulses required by the target devices. The *trigger pulse generator*, which converts the pulse width, and the E/O converter module are used optionally.

These modules have been designed, built and tested. The timing control softwares and GUI are now under developing.

SYNCHRONIZATION TIMING

The synchronization timing is defined as timing signals based on the trigger generated by the accelerator device other than the central timing control. The synchronization timing is necessary for the devices which needs to be synchronized with the real beam, while most devices of the J-PARC are operated with the scheduled timing.

The following devices uses the synchronization timing.

- The beam chopper in the linac works with the chopping signal generated and sent from the RF system of the RCS so that the beam is injected into the center of the RF bucket of the RCS.
- The extraction kicker of the RCS and the injection kicker of the MR fire based on the trigger from the RCS RF system to be synchronized with the real circulating beams in the RCS.
- The neutrino experiments use the RF clock of the MR.

The optical fiber connections for the synchronization timing signals have peer-to-peer architectures. The scheduled and synchronization timing systems work cooperatively and complementary to each other.

NON-SYNCHRONIZED OPERATION TO AC-LINE

The scheduled timing system works based on the 12 MHz master clock generated by a high-stability synthesizer. The 50 Hz trigger clock is generated by counting the master clock; thus the system is not to be synchronized with the AC-line frequency. Scheduled extraction from the RCS in a fixed period simplifies the synchronization between the RCS beam and the Fermi chopper, which has a

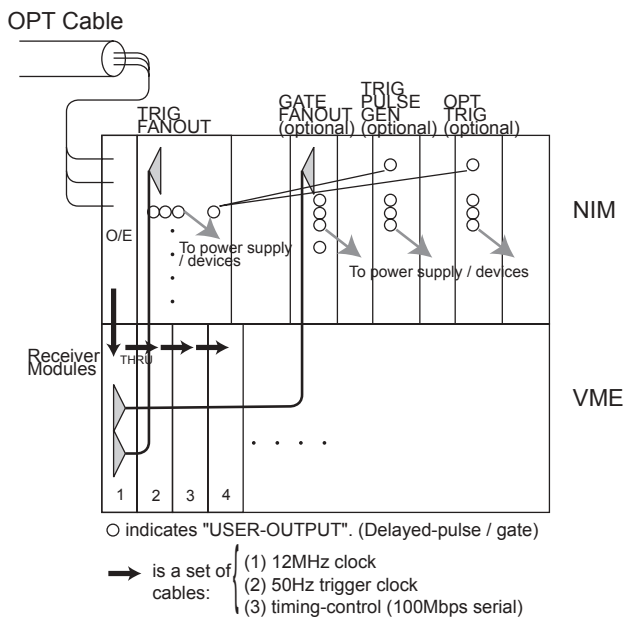

Figure 2: Timing receiver panel.

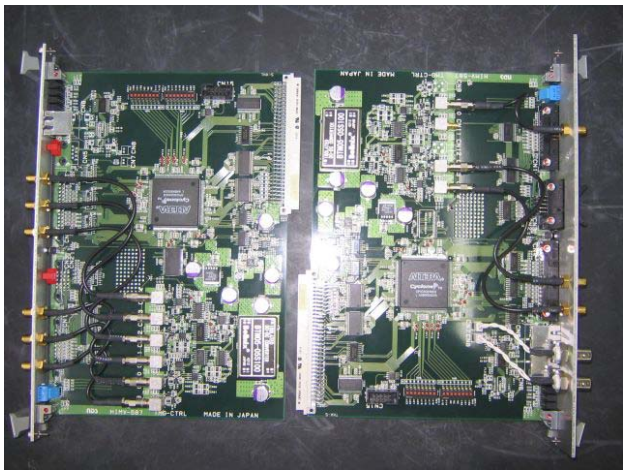

Figure 3: The timing control transmitter (right) and receiver (left) modules.

Figure 4: The timing control receiver modules in mass production.

small tolerance of 100 nsec (Note that the tolerance consists of the chopper jitter and the beam jitter), in the MLF. The RF synchronization of the RCS to the MR is much easier with the fixed period extraction. Furthermore, the RCS magnet network has high Q-value ($\sim$100); the tracking become difficult if the RCS cycle varies.

However, there are possible impacts if the accelerators are not to be synchronized as follows.

- Power supplies with thyristors are generally more stable with AC-line synchronization.
- The linac RF sources are easy to be influenced by the voltage ripples.
- Monitor signals can be affected by the 50-Hz AC line. If the accelerator is "non-synched", the measurement itself may fluctuate by the beating noise and the S/N becomes worse.

Figure 5: The transmitter and receiver modules under testing.

In the synchrotrons, switching power supplies are mainly used and the effect of the AC-line is minimum. Also, the linac RF has precise feedback system to stabilize the RF amplitudes. Thus, these issues are considered to be managed.

The examination of the non-line-synched mode is to be done with the real beam operation.

SUMMARY

We summarize the presentation as follows.

- J-PARC requires the stable timing system to manage the high beam power.
- Two kinds of timing, *scheduled timing* and *synchronization timing* are defined for the J-PARC.
- the three accelerators (linac, RCS, MR) have the different repetition rates.
- The scheduled timing system realizes the different operations every 50Hz period.
- The synchronization timing is based on the trigger generated by the accelerator device other than the central timing control.
- The timing system works without AC-line synchronization.

REFERENCES

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